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Future of plasma etching for microelectronics: Challenges and opportunities

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ABSTRACT

Plasma etching is an essential semiconductor manufacturing technology required to enable the current microelectronics industry. Along with lithographic patterning, thin-film formation methods, and others, plasma etching has dynamically evolved to meet the exponentially growing demands of the microelectronics industry that enables modern society. At this time, plasma etching faces a period of unprecedented changes owing to numerous factors, including aggressive transition to three-dimensional (3D) device architectures, process precision approaching atomic-scale critical dimensions, introduction of new materials, fundamental silicon device limits, and parallel evolution of post-CMOS approaches. The vast growth of the microelectronics industry has emphasized its role in addressing major societal challenges, including questions on the sustainability of the associated energy use, semiconductor manufacturing related emissions of greenhouse gases, and others. The goal of this article is to help both define the challenges for plasma etching and point out effective plasma etching technology options that may play essential roles in defining microelectronics manufacturing in the future. The challenges are accompanied by significant new opportunities, including integrating experiments with various computational approaches such as machine learning/artificial intelligence and progress in computational approaches, including the realization of digital twins of physical etch chambers through hybrid/coupled models. These prospects can enable innovative solutions to problems that were not available during the past 50 years of plasma etch development in the microelectronics industry. To elaborate on these perspectives, the present article brings together the views of various experts on the different topics that will shape plasma etching for microelectronics manufacturing of the future.

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I. INTRODUCTION

Plasma-assisted etching has been one of the key technologies that has enabled the unparalleled progress of the microelectronics industry over the last 50 years, advancements that are often described as Moore's law. As first noted by Moore,[1] exponential progress in the capabilities of microelectronic circuits can be achieved by geometric reduction of semiconductor devices and components, appropriate device and circuit scaling, and larger die sizes. These strategies enable packing more semiconductor devices on a silicon chip, thus realizing an economic benefit. To enable the production of smaller scale devices that could not be made using isotropic wet etching methods—and help maintain Moore's law from micrometer to ultimately nanometer scale dimensions—plasma etching (PE) was introduced into the microelectronics industry in the 1970s.[2] Essentially, PE is an approach for transferring lithographically defined resist patterns into the materials forming integrated circuits in a directional and material selective manner in a gas plasma environment. The materials were at first primarily silicon, silicon dioxide, Si_3N_4, and aluminum, but recently have expanded to many elements of the periodic table. During these 50 years, plasma etching has evolved dynamically along with photolithography and thin-film deposition methods to enable the sustained realization of an exponential increase in performance per unit cost of the semiconductor industry over time. This economic benefit has made a major impact on the world at large by providing the technological foundation of the digital revolution and information age.

After entering the new century, traditional semiconductor scaling approaches[3] have been challenged to provide satisfactory solutions for increasing the performance of integrated circuits.[4] The conventional methods have been augmented by the introduction of new materials, 3D device architectures, quantum devices, and other approaches. The vast growth of the microelectronics industry must now also address major societal forces, including questions on the sustainability of the associated energy use, emission of greenhouse gases, and other factors. Addressing these challenges will influence the production of semiconductor devices and circuits, and microelectronics processing methods in general.

The future of plasma etching for microelectronics will be driven by several issues, including the evolving manufacturing needs of the semiconductor industry as fundamental silicon device limits are approached, workforce constraints of the semiconductor industry, the transition to more sustainable practices and meeting legislative environment regulations, and what can be done economically in the technology space. Since there are many unknowns with regard to the technology paths, regulatory environment, and economic factors, a definite description of all aspects of plasma etching of the future is not possible. The goal of this article is to help define scientific challenges for plasma etching and point out effective plasma etching technology options that may play essential roles in future microelectronics manufacturing. The novel challenges are accompanied by significant new opportunities. We will show that new techniques, including integrating experiments with various computational approaches, such as machine learning (ML)/artificial intelligence (AI), and the realization of digital twins of physical etch chambers through hybrid/coupled models, can enable innovative solutions that were not available during the past 50 years of etch development in the microelectronics industry. To elaborate on these perspectives, the present article brings together the views of various experts on the different topics that will shape plasma etching for microelectronics manufacturing of the future. These contributions will briefly review the status and point out the needs and opportunities of these areas.

The path forward for plasma etching technologies will be shaped by a combination of disruptive and continuous innovations that take place in parallel that are capable of manufacturing the required, but as yet not defined, semiconductor products of the future, while meeting the sustainability requirements of future society. This article attempts to clarify critical aspects of this transition, which will require the integration of several disciplines and approaches. This integration is shown schematically in Fig. 1, which provides a pictorial view of how the topics addressed by the subsections of this article come together to review essential aspects of the required transitions.

We begin with several industrial perspectives, including plasma etching needs based on expected device and circuit evolution. Multiple plasma etching processes take place in a highly refined sequential process sequence that produces the final microelectronics product. The impact of the recent introduction of direct print extreme ultraviolet (EUV) pattern transfer on plasma etching

processes for a specific application is reviewed next. Exemplary considerations required for co-optimization of a plasma etching step with the overall process integration flow are then described.

Next, plasma etching challenges connected with complex 3D structures, including high-aspect-ratio (HAR) processing of insulators and conductors, are reviewed. Sustainability considerations including green chemistry and environmental issues connected with chemical precursors and emissions that will shape plasma etching chemistries of the future follow. Post-CMOS (complementary metal–oxide–semiconductor) evolution may require new structures and material functionalities, which will need more complex materials sets. Special considerations associated with plasma etching of these, including those with involatile etching products, are introduced.

This is followed by the viewpoints of experts from three major plasma etching equipment suppliers on future plasma etching needs for microelectronics along with visions of new approaches that could realize that technology.

A number of recent innovations will likely have a direct influence on accelerating the resolution of these long-standing PE challenges, and these opportunities will be highlighted. These include improvements in our basic understanding of plasma-surface interactions of dry-etching processes, the role of plasma-generated ultraviolet (UV), and vacuum ultraviolet (VUV) radiation at surfaces and doping effects. The control of surface processes benefits from approaches such as atomic layer etching (ALE) that enables ultra-high materials etching selectivity and plasma cryogenic etching for material selectivity and rate control. Improved control of semiconductor PE can be achieved using real-time diagnostics and metrologies, and machine learning provides new ways of dealing with and advancing research and development and more effective process monitoring of plasma etching. Finally, advanced reactor and

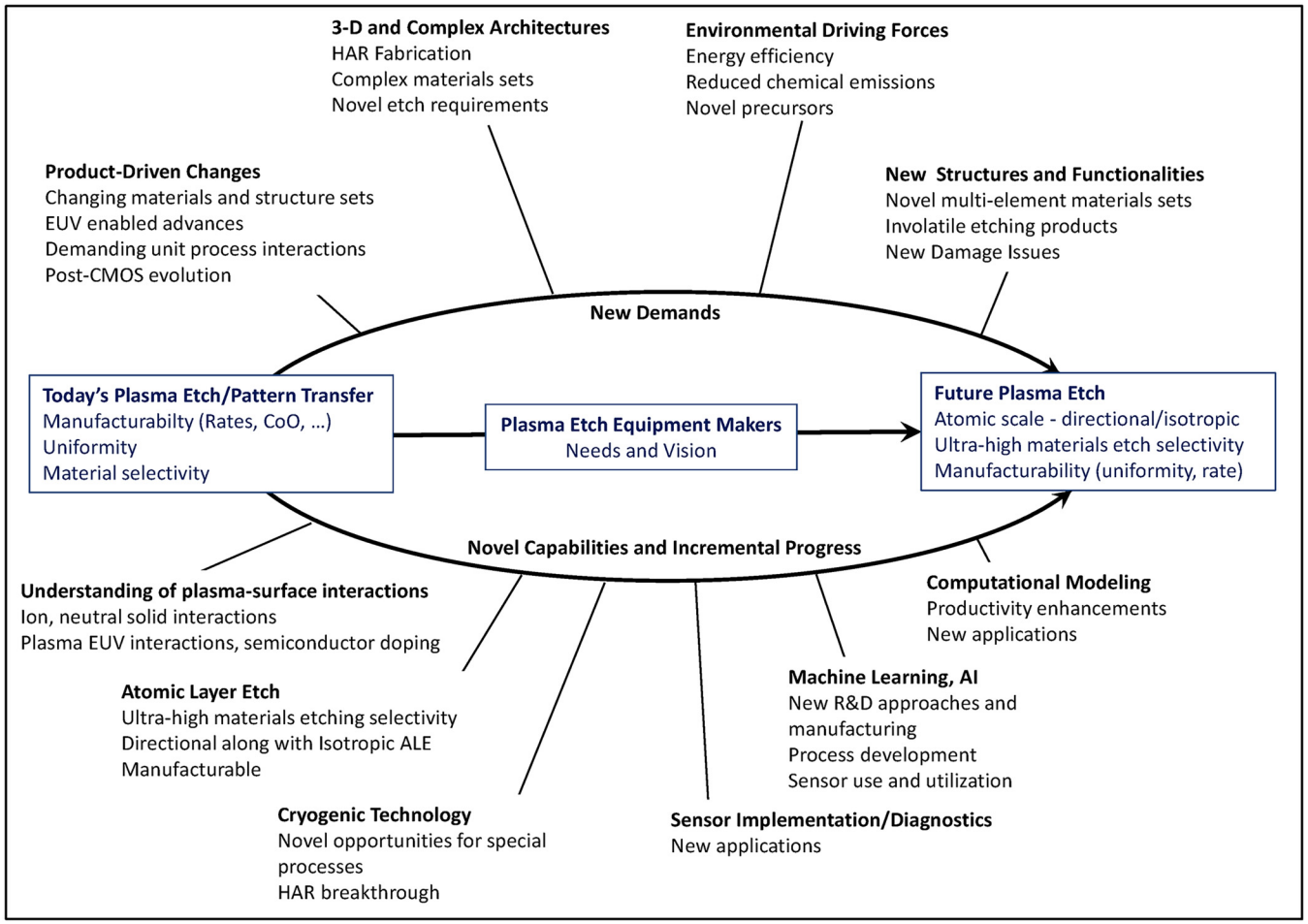

FIG. 1. Overview of driving forces and processing challenges that will affect plasma etching of the future. Novel capabilities along with incremental progress will meet these challenges. The vision of plasma etch equipment suppliers on manufacturing needs and possible approaches adds to these requirements.

feature-scale computational modeling have greater power than ever before for directly influencing the conception, design, and manufacturing of actual plasma reactors and processes for atomic-scale control of etched features, and they are described in Sec. II P.

There are important challenges in PE that this article has chosen not to address in detail. For example, to further leverage modeling and computer simulation in PE development, the development of chemistry databases of plasmas/gases, including both electron-impact and heavy-particle processes, the necessity of surface sticking coefficients, surface reaction rates and interatomic potentials in surface modeling, and the control of error propagation in multiscale simulations are highly desired. Many of these needs and challenges are only briefly mentioned in the subsections of this article and should be kept in mind, even though they were not selected for descriptions that are more detailed.

II. CHALLENGES AND OPPORTUNITIES FOR REALIZING PLASMA ETCHING OF THE FUTURE

A. Industrial perspectives of plasma etching needs in the future

Robert L. Bruce, Chanhoon Park

1. Status and promising developments

Plasma etching has been an integral part of the pattern transfer process in the semiconductor industry for more than 50 years. The advancements in plasma etch technologies in part enabled the continuous shrinking of device critical dimensions (CDs), allowing the exponential increase in transistor and memory densities. However, it is not only the areal device densities that have changed in the recent decade but also the evolution of planar to 3D device architectures,[5,6] including the stacked gate-all-around (GAA) devices in logic and 3D-NAND devices in memory. Patterning these complex structures has brought even more innovations to plasma etching.

In general, the industry has adopted EUV lithography as the successor to 193i and deep ultraviolet (typically 200–280 nm) lithography to push below 40 nm pitch features for the 5 nm technology node and beyond (see Sec. II B). While EUV at a single exposure (SE) (readily achieves dimensions that require multiple patterning strategies with 193i lithography, the EUV light source is weak (14× less photon yield compared to 193i) and the photoresist (PR) suffers from low mechanical strength, low sensitivity, and line-edge roughness/line width roughness (LER/LWR) and poses a challenge for pattern transfer by plasma etch.

The EUV PR is among the many newly introduced materials in the semiconductor industry that require atomically precise and low damage etching methods. ALE (see Sec. II L) is an approach to achieve atomic level precision in pattern transfer and selectivity by separating reactant adsorption and etching cycles and controllably removing a layer of material at a time. Other novel etching approaches are also being explored. Electron beam-generated plasmas[7,8] are being employed in several methods to minimize the impact of energetic ions. Neutral beam etching[9] has shown promise by inserting a carbon plate with apertures between plasma and reactor and filtering the ions and VUV irradiation. Etching and surface treatment by radicals[10] have recently been reported by flowing a reactive chemistry below an inert plasma and generating reactive radicals with ultralow energy.

The evolution of the field-effect transistor (FET) device from planar to fin to gate-all-around has driven much innovation in plasma etching technology. The cutting edge of 2 nm technology node and below is displayed in Fig. 2 schematic of a vertically stacked gate-all-around structure with self-aligned contacts to source/drain (S/D) regions and back-end-of-line (BEOL) metal interconnects.[5,6]

About a decade ago, 3D-NAND replaced the planar architecture and has continued showing success as word-line stacking that started at 24 layers has reached now over 400 layers.[11] However, etching the high-aspect-ratio memory stacks has become increasingly difficult (see Sec. II D).

2. Unresolved issues and challenges

Much of the work to improve plasma etching is to maintain pattern fidelity, increase material selectivity, and avoid plasma-induced damage (PID) (see Sec. II G). Added to these tasks are patterning an expanding list of new materials systems (see Sec. II H) and etching through many device elements stacked in the z-direction. There are many plasma etching challenges in the semiconductor industry, but in this section, we will focus on four key issues: EUV PR patterning, low damage etching of novel materials systems, beyond Cu interconnects, ALE for self-aligned contacts, and high-aspect-ratio contact (HARC) etch innovations for memory applications.

Several strategies can be used to overcome poor pattern fidelity and insufficient PR selectivity in state-of-the-art EUV PR systems. One strategy is plasma treatment using CS gas as shown by Chang

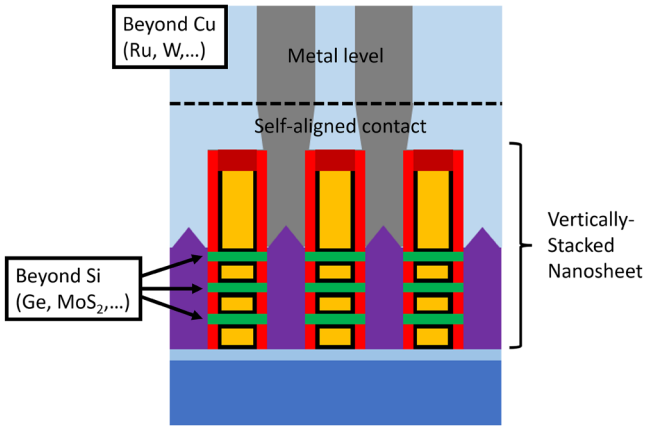

FIG. 2. Schematic of the vertically stacked gate-all-around architecture at 2 nm technology node. Future logic devices are being investigated with replacement of Si channel (beyond Si) and Cu metal level (beyond Cu) potentially for below 2 nm technology node.

et al.,[12] where S penetration improved LER via PR surface hardening and smoothing, thus creating additional C=S and S=O bonding. Other sulfur-containing gases (H_2S, COS, SF_6, etc.) are also being considered to improve patterning performance. Another strategy is the area selective deposition (ASD) approach, which is a cyclic deposition and etching process. For the deposition step, conventionally a hydrocarbon forming gas such as CH_4 is used as a precursor; newer approaches use atomic layer deposition (ALD) precursors such as bis(T-butylamino)silane or di-isopropylamino silane. Preferential deposition occurs on the PR, and subsequent ASD cycles result in little PR loss during etch of the underlying layer. The ASD approach, however, is slow, and finding the optimal deposition/etch cycles while minimizing process time is essential. Many ASD processes have been published,[13–15] and new research has been reported to further improve EUV PR patterning with vapor phase infiltration.[16]

The applications for low damage etching are growing as materials systems have become more challenging to pattern. For example, the technological outlook for two-dimensional (2D) materials in future devices is promising. Graphene and carbon nanotubes are being considered in transistors, interconnects, and sensors, and electron beam generated plasmas have shown advantages in reducing patterning damage to these materials.[17] MoS_2, WSe_2, and other transition metal dichalcogenide materials are being looked at as next-generation transistors and layer-by-layer MoS_2 etching has already been demonstrated through an ALE approach.[18] Low-k dielectrics are used to reduce the parasitic capacitance in interconnects at the extreme scale by adding porosity to the dielectric, leading to increased sensitivity to plasma damage during patterning. Cryogenic etching (see Sec. II N) has been demonstrated to reduce plasma-induced damage.[19] Chalcogenide-based phase change materials and selector materials may be used in next-generation memory concepts such as analog AI and storage class memory. However, the specific elemental stoichiometry must be maintained for proper functioning in these multielement alloys, and plasma-induced damage that causes elemental redistribution and oxidation/reduction reactions must be addressed.[20] Strategies to enable halogen-free plasma etching and postetch encapsulation without vacuum break have been shown to reduce plasma damage.[20,21]

Interconnects have driven much innovation in the development of dielectric etching since the establishment of the Cu damascene process ~25 years ago.[22] As we continue scaling below 15 nm metal linewidths, Cu begins to exhibit increasingly larger resistances that considering several metals discussed below at the same dimension becomes a desirable option.[23] Additionally, the requirement of a Cu diffusion barrier liner is independent of linewidth, so that the actual Cu dimension becomes smaller compared to using another metal with different diffusion properties.[24] The damascene approach itself is tailored to Cu integration since Cu is extremely difficult to dry etch due to the formation of nonvolatile halogen byproducts.[24] Choosing alternative metals opens the possibility of returning to subtractive etching of interconnects. Alternative metals being considered using subtractive etching include Ru, W, Mo, and Nb.[25] Since Ru readily etches in an O_2-based plasma, there has been much work evaluating it as the next interconnect metal.[25,26] Due to high volatility of RuO_4, the postetch surface of Ru is relatively oxide free, which can be a challenge for other metals such as W, Mo, and Nb.[25] Co, Ir, and Rh also show promise as low resistivity options; however, dry-etching proves as challenging in these metals as for Cu.[27] A Co chemical vapor deposition (CVD) process has been developed and integrated,[28] but very little has been reported in the literature for Ir and Rh etching.

Further down the line, a novel material called a topological semimetal might be in future interconnects. Topological semimetals show the interesting property of continuing to decrease in resistivity going below 15 nm linewidth as compared to conventional metals due to their surface states dominating current conduction.[29] Various alloys, such as CoSi, NbAs, TaAs, TaP, and others, are being investigated, but there has not been much reported in the literature of patterning and integration of topological semimetals.[30]

Over the past decade, atomic layer etch (ALE) has been put to use in the semiconductor industry and the self-aligned contact (SAC) etch is one process that has significantly benefitted from the ALE approach.[31] SAC etch is a source/drain (S/D) contact patterning scheme that addresses misalignment by leveraging the etching selectivity between the contact dielectric and gate spacer when etching down to the S/D region. In sub-7 nm logic devices, ALE has been essential to minimize low-k SiN_x spacer loss when opening an SiO_2 contact dielectric. In the deposition step, the polymer is deposited thicker on the SiN_x spacer than SiO_2 and in the activation step, the difference in thickness of the deposited polymer is used to etch SiO_2 without etching the SiN_x spacer. The selectivity of this process improves with increased deposition-activation cycles, but throughput suffers. The industry has responded by developing equipment improvements to reduce the transition time between ALE cycles (fast gas transition, fast plasma ignition, stabilization, etc.) and better control of the ion energy.

Further challenges are described in the memory industry. While continued device scaling has improved memory performance, etching HARCs, such as VNAND channel holes and dynamic random access memory (DRAM) capacitors has become increasingly difficult. The main challenges are depth loading due to ultrahigh aspect ratios and the 3D effect as lateral pitch size decreases. The conventional approach for etching HARC structures has been to increase the ion energy reaching the etch front, achieved by employing a higher power, lower frequency (≤600 kHz) radio frequency (RF) bias generator and using direct current (DC)-like rectangular pulses. However, challenges remain due to mask clogging and generator arcing issues, which can be mediated by reducing the RF bias duty cycle, though wafer throughput suffers (Fig. 3).

As will be discussed in Sec. II N, cryogenic etching is a newer strategy that focuses on maximizing the radicals transmitted to the etch front. The first-generation of cryogenic etching uses (a) a large amount of hydrogen carrier gas to react on the dielectric surface, reducing C_xF_y, CH_xF_y, and halogen gas compared to the conventional method, which limits mask clogging and (b) cryogenic temperatures (≤−20 °C), which lead to more HF-related species adsorption at the etch front. However, since the first-generation approach still uses a carbon-containing gas mixture, the problems of mask clogging, profile deformation, and depth loading remain a concern. The second generation of cryogenic etching eliminates the need for carbon-containing gases by directly employing HF gas. Combined with a catalytic gas containing fluorine, used to

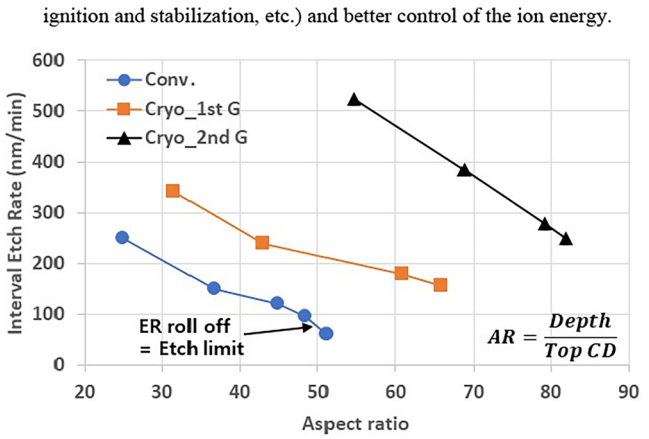

FIG. 3. Interval etch rate vs aspect ratio of conventional and cryogenic first/second generation etch. Cryogenic etch improves etch throughput and achieves much higher aspect ratios.

accelerate the surface reaction, the etching time is reduced for a ~60:1 aspect ratio (AR) structure by ~50%.[11] Currently, the direction of HARC etch process development for next-generation devices is to combine the approaches of optimal etch chemistry (including catalyst gas) and environment (wafer temperature, radical density, ion energy/density) rather than applying more bias power.

In this section, we reviewed the etch innovations introduced to pattern leading edge logic and memory technologies. In logic, we continue to march further down the path of metal–oxide–semiconductor field-effect transistor scaling and ultimately toward beyond CMOS concepts. The industry is already exploring smaller scaling by stacking n-MOS and p-MOS gate-all-around devices in a self-aligned patterning approach.[6] Also, in order to achieve even lower power operations, beyond CMOS concepts are being explored, such as negative capacitance FETs, tunnel FETs and spin-FETs, bringing new types of materials (e.g., 2D materials, multicomponent alloys, superlattices), and architectures for etching.[6] Therefore, it is essential to understand processes at the atomic level to achieve the level of precision currently required and this can only be realized by continued close collaboration between industry and academia.

B. Direct print EUV pattern transfer using plasma etch for tight pitch metal layers

Hiten Kothari, Steven G. Jaloviar

The adoption of EUV lithography has been introducing new challenges for pattern transfer by plasma etching. We describe the pattern transfer for direct print EUV layers using plasma dry etch for tight pitch metal layers. Careful co-optimization of the lithographic process, film stack, and etch processes is necessary to deliver a defect-free process window for high-volume manufacturing (HVM). The etch process needs to be optimized for the entire stack, including resist, underlayer, and carbon hardmask film, to provide the best overall process. Stack material selection is critical for optimizing the etch parameters and conditions for process transfer. We describe that the use of special test masks specifically designed to increase the sensitivity of key defect modes on the defect metrology tools is helpful to quicken the speed of development. Electrical and yield results based on the defectivity measurements demonstrated achievement of HVM readiness.

1. Overview

Advances in lithography and integrated process technology have enabled continual Moore's law scaling by shrinking the minimum resolvable pitch for decades. Immersion lithography with double and quad patterning has been extensively utilized to extend the pitch scaling until EUV source, resist, and mask technologies were ready. Today, EUV lithography is used for high-volume manufacturing in advanced nodes for patterning critical layers up to 35 nm. Below 35 nm, EUV lithography is often paired with complicated integrated processes such as self-aligned litho-etch litho-etch (SALELE) for the most critical layers. In the industry, direct print EUV technology is being used up to 30 nm to reduce process complexity and cost. This paper describes how etch innovations can enable tight pitch line-space patterns with flexible design rules using direct print 0.33 numerical aperture (NA) EUV.

The overall advantages and challenges of direct print patterning as compared to SALELE are discussed at length by Venkatesan *et al.*[32] SALELE continues to be a popular choice in the industry for pattern transfer below 35 nm and has been demonstrated to work down to ~24 nm pitch. Here, we aim to cover etch challenges associated with the tight space direct EUV pattern transfer and the key defect modes that limit the process window. Primary defect modes that need close co-optimization are shorting modes from fallen lines and broken mesa and opens mode from blocked etch leading to microbridges also referred to as minis in this section. Resist selection with the right underlayer and the associated stack to minimize these defects is key. Etch processes need to be optimized and developed to deliver the pattern transfer with minimal defects and with low dose resist at EUV lithography to minimize the process cost.

2. Resist and underlayer selection

A general stack for pattern transfer is shown in Fig. 4. Chemically amplified resists (CARs) are primarily used today for

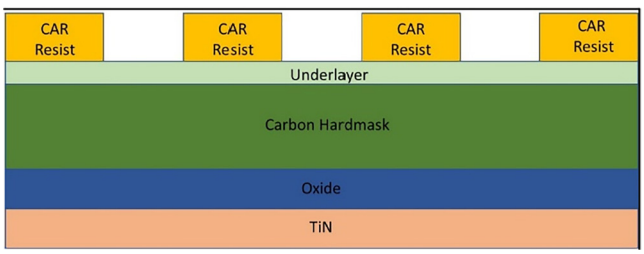

FIG. 4. General stack for pattern transfer.

EUV patterning. The ideal resist will provide a square profile, low LWR, low dose for patterning, good process window against fallen lines, and minimum scumming/residue defects while providing adequate thickness for pattern transfer during underlayer etch. A higher thickness of resist post development is desired for transfer etch but can be challenging for fallen lines process window.

Underlayer selection is critical to the resist and needs to be optimized for the resist in question. EUV lithography does not require antireflective coatings for the underlying film, allowing for additional options for underlayer selection. Additionally, the underlayer film needs to be optimized to withstand the carbon hardmask etch. Spin-on underlayers have historically been the norm for line/space (L/S) patterning layers. For tight pitch L/S patterning, thin-film-based underlayers using ALD/CVD have shown an improved lithographic process window for the resist and the benefit of this approach was quickly evident. From an etch perspective, high selectivity to CAR for underlayer etch is critical. Subsequently, the carbon hardmask etch needs to be selective to this underlayer. Figure 5 shows the key defect modes that need to be addressed for a good process window. Figure 6 highlights the impact of the underlayer on the fallen line defect density. Thin-film deposited underlayers were found to be superior for fallen lines defect density compared to spin-on underlayers. An exponential increase in defect density is evident as the pitch is reduced.

3. Descum and underlayer etch

While fallen lines are governed by lithographic processing, microbridges and broken mesas defect mode can be modulated by the etch process. Microbridges lead to chain fails for yield while broken mesas lead to shorts for yield. Optimization of the process is done using specially designed test vehicles with high visibility on commonly used defect metrology tools to these defect modes. There are two prime sources for the microbridge defect. The primary mode is residue postlitho processing and the second one is particles from different tools and layers in the processing flow. Microbridges are extremely elevated without a descum step at etch to remove the residue between the trenches, confirming that the primary source of microbridges is incoming to the etch process. Here, descum refers to the removal of residues (scum) from the substrate, e.g., by plasma cleaning. The residue is understood to be underdeveloped resist or the redistribution of byproducts adhering to the underlayer, making it challenging to remove these defects while still retaining enough resist for pattern transfer. The removal of this residue is done using

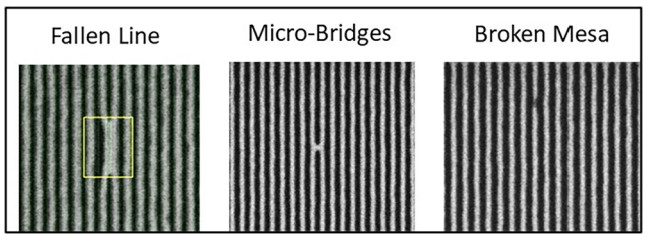

FIG. 5. Representative image for key defect modes.

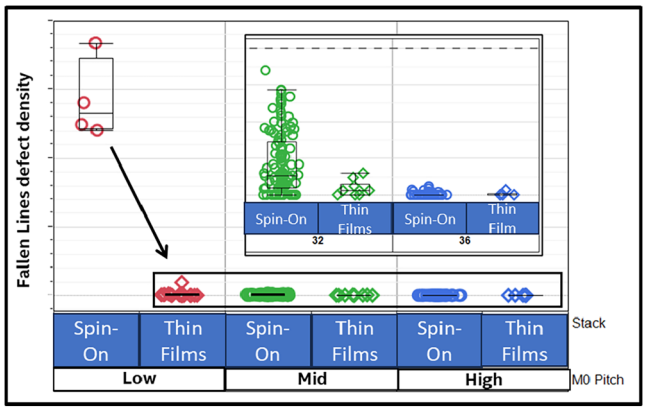

FIG. 6. Impact of underlayer deposition method on fallen lines defect density.

a descum step. Optimization of this descum step is critical to the overall process window. If the descum is too aggressive, lack of resist protection leads to broken mesa. If descum is too gentle, it is not effective in cleaning up incoming defects.

Figure 7 highlights the impact of different descum chemistries on the overall microbridges performance. As the descum chemistry gets more aggressive, the mini defect modes reduce. The aggressiveness of the descum increases going from N_2 based plasma to H_2/N_2 based plasma. The defect level does not drop meaningfully until a fluorinated chemistry is used for residue removal. Additional optimization of the fluorine-based chemistry provided a significant reduction in defectivity while minimizing overall resist loss and improving the process window. Additionally, the overall mini defect counts are insensitive to CDs when the descum etch is

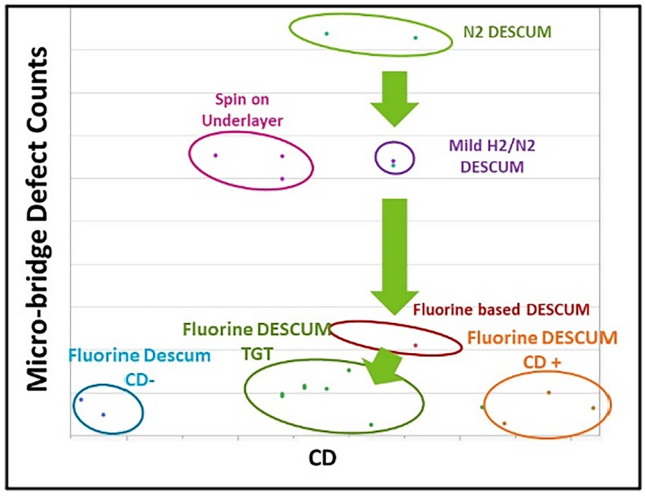

FIG. 7. Impact of descum on the microbridges defect mode for fine pitch L/S EUV patterning.

correctly optimized. The actual range of CDs is considered proprietary and has not been listed.

Following the descum step, the underlayer etch needs to be completed with minimal resist loss to prevent shorting modes and maintain a straight profile through the underlayer. Chemistry selection plays a critical role in this etch. As such, significant optimization is needed for the etching chemistry, and RF parameters, pressure, and gas flow are selected for optimal etch. Recent advances in multistate RF pulsing have been shown to provide additional process control for etching.[33] Taking advantage of these new capabilities, end-pointed underlayer etches have been developed to enable good selectivity while maintaining excellent process control, defectivity, and profiles.

The secondary source of mini defects is small particles or impurities in the material stack that cannot be removed by the descum step. The impact of these defects increases with smaller pitches. A novel directional tip-to-tip (TTT) etch process is used to selectively clean the microbridges within the trench without affecting trench CD. Here, TTT is defined as the distance between line ends. It is also commonly referred to as tip-to-tip CD in the metrology of features. To minimize the CD expansion of the trench, the film property of the carbon hardmask etch is tuned to provide more etch resistance as shown in the left plot. The End-To-End (ETE) etch process reduces process complexity and cost by eliminating an EUV cut mask but also helps to reduce defectivity as shown in the right plot of Fig. 8.

4. Summary and outlook

Patterning tight pitch line-space patterns at the resolution limit of the lithography scanner requires careful co-optimization and a holistic patterning development effort. As highlighted here, lithography, thin films, and mask technology along with plasma etching expertise need to be co-optimized for a reliable, high yielding, cost effective, and manufacturable process.[32] The characterization and design of photoresist properties and purity is critical to prevent stochastic defects from the photoresist while simultaneously enhancing etch resistance. The careful choice of underlayers can allow optimal etch transfer and significant photoresist profile improvements. All these factors will continue to be optimized as we continue to shrink the pitch and feature sizes according to Moore's law. High-NA EUV lithography will be even more important as minimum pitches scale lower. High-NA EUV at tighter pitches will have a lower depth of focus requiring thinner resist thickness, further challenging the pattern transfer etch. Advancement in material systems, stacks, and new etch technology will be crucial to keep advancing Moore's law.[34,35]

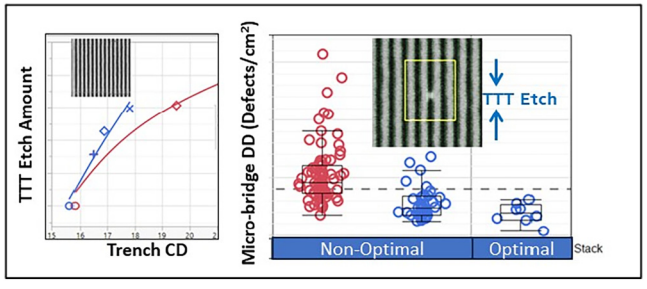

FIG. 8. Novel TTT push capability.

C. Plasma etching co-optimization with the process integration flow

Theo Standaert, Eric Miller

1. Overview

Today's computer chips are manufactured in state-of-the-art fabs where silicon wafers traverse a complex process sequence through a large set of advanced semiconductor equipment. These steps are counted by the hundreds if not thousands for the most advanced chips and include processing, metrology, inspection, and electrical testing. To optimize performance and yield, these steps are all highly co-optimized and reused as much as possible from prior technology nodes to expedite time-to-market.

Plasma etching is a powerful approach used in the semiconductor process flow to transfer or shape patterns onto the wafers. Figure 9(a) schematically shows a small portion of the integration flow where the blue dot represents a plasma etching step. Since this step helps to define the patterns on the wafer, there are important interdependencies to be considered with downstream [Fig. 9(b)] and upstream process steps [Fig. 9(c)]. Figure 9(d) schematically depicts a much more complex process integration flow where a single pattern is transferred using multiple photolithography and plasma etch steps. These visualizations are meant to sketch the process interactions and process window complexities, which will be discussed next.

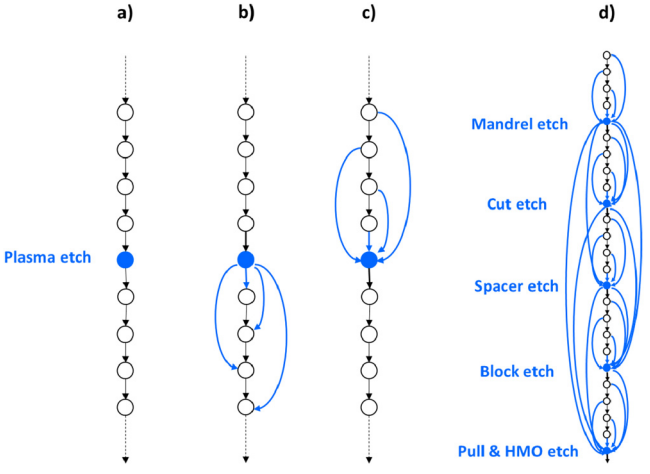

FIG. 9. Schematic of a portion of the integration flow with plasma etch step represented by the blue dot in (a). The downstream and upstream dependencies are shown by the blue arrows in (b) and (c), respectively. Finally, the process complexity for a dual patterning flow as discussed by Sun *et al.* (Ref. 39) is illustratively captured in (d).

2. Status and promising developments

The BEOL or interconnect process integration flow is a good example to highlight the process interactions with plasma etching. BEOL must deliver on three key metrics, which are typically in competition with each other: yield, reliability, and minimizing the resistance and capacitance (RC) delays. For conventional Cu interconnects, a bilayer liner is deposited onto the etched feature first. The materials and thicknesses of the liner stack are chosen to obtain an excellent Cu diffusion barrier and adhesion between Cu and the interlayer dielectric (ILD).[36] Figure 10(a) shows a sketch of an etched trench into the ILD with a TaN/Co liner bilayer. TaN is typically deposited using physical vapor deposition (PVD) and inherently has a bread loaf shape near the feature opening resulting in a thinner film in those areas that have reduced line of sight to the ionized species. The Co film has high conformality since it is deposited by CVD. The bilayer liner is then followed, all *in situ*, by a PVD Cu seed film, which also has bread loafs near the opening. Even with an ideal profile as sketched in Fig. 10(a), it can be challenging for tight pitch configurations to find a process window where the liner and seed films are thick enough on the feature sidewalls while still leaving enough of an opening at the top of the feature to plate through. Figure 10(b) shows a high angle annular dark field scanning transmission electron microscope (STEM) image of a 48 nm pitch interconnect where small voids are visible near the sidewalls. The prewet step during Cu plating is designed to first remove the native Cu oxide and will galvanically attack the underlying Co if the original Cu seed is too thin on the sidewall. These Cu voids then result in a fast Cu electromigration path and significantly reduce the interconnect lifetime. It is, therefore, paramount to optimize the plasma etching and produce a feature that is friendly for the PVD processes that follow.

The etched profile gets more complicated in Fig. 11(a), which shows a dual damascene V1/M2 profile landing on M1. The etch stop and hardmask are each depicted as a single layer, but it should be noted that they can consist of multiple films. The ILD in Fig. 11(a) is undercut below the hardmask and extremely challenging to cover with PVD liners. Hence, much thicker liners would be required to cover this corner at the expense of RC or, alternatively, a penalty in yield and reliability due to defects in these corner regions.[37] A second example is shown in Fig. 11(b) where the hardmask has been chamfered—removal of the sharp edges of a feature—to eliminate the undercut and obtain a profile that is optimized for Cu metallization. The hardmask chamfer can be obtained during plasma etching by, for example, deploying higher ion energies and reducing the selectivity to the hardmask. However, the via profile parallel to the trench is unprotected and will also chamfer, resulting in a larger bottom CD. This in turn raises the risk of dielectric breakdown and even shorting to the underlying M1. A more attractive and demonstrated solution for multiple technology nodes is to selectively remove the hardmask prior to metallization as depicted in Fig. 11(c).[37,38]

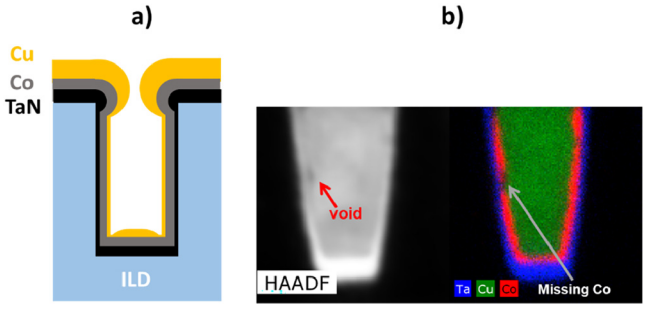

FIG. 10. Etched feature followed by a bilayer TaN/Co liner and Cu seed is sketched in (a). A 48 nm pitch interconnect with void defects is shown in (b).

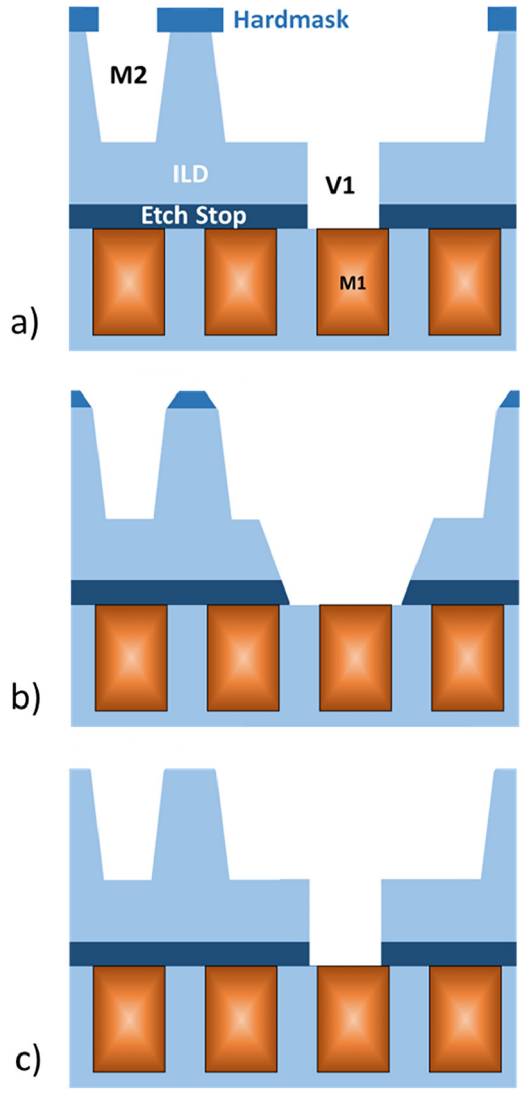

FIG. 11. Three dual damascene profiles: (a) has undercut near the hardmask, (b) has undercut chamfered away, and (c) has the hardmask selectively removed.

The examples above clearly demonstrate how plasma etching must be co-optimized with downstream process steps. This is schematically captured by the blue arrows in Fig. 9(b). Of course, plasma etching must also be co-optimized with upstream processes such as film depositions and photolithography. These upstream dependencies are captured in Fig. 9(c). A practical example is shown in Fig. 12(a) where a one-meter-long comb-serp yield is plotted as a function of a hardmask film thickness during early development stages of a 36 nm pitch BEOL using SE extreme ultraviolet (EUV) lithography.[38] The dashed green target line and red spec limits for the hardmask deposition were reused from the prior technology node. The yield varies strongly within this window and is primarily gated by a single line opens defect shown in top-down and cross section in Figs. 12(b) and 12(c). In this case, the process window was significantly improved after recentering and tightening process controls for both hardmask deposition and plasma etching. A yield of nearly 100% was achieved through additional co-optimization with other upstream processes. Such co-optimization can be nontrivial and patterning, including photolithography and plasma etching, is often pivotal to establish a common process window across the integration flow.

The overall process complexity takes an enormous leap when multiple photolithography and plasma etching steps are required to form a damascene level. For example, self-aligned double patterning (SADP) doubles the pitch that is printed, but additional passes through photolithography and plasma etching are then required to make cuts or blocks and obtain the final design layout on the wafer.[37,39] To put it differently, a complex sequence of multiple photolithography and plasma etching steps are combined with many other processing steps to assemble the design into a hardmask before it finally gets transferred into the ILD. The result is a complex pattern assembly where multiple plasma etching steps must be simultaneously co-optimized with the other processing steps as illustrated in Fig. 9(d). This level of complexity requires significant engineering investments along with tight process controls and advanced feedback loops. Even when the pattern assembly looks great on the wafer during early development stages, further optimization will be required to reduce defects and achieve yield targets. An example is shown in Fig. 13(a) where the final pattern assembly into the hardmask looks great, but one of the trenches is blocked by a defect. This defect then interferes with the subsequent plasma etching step into the ILD and manifests as a single line open after Cu chemical mechanical polishing in Fig. 13(b). The STEM analysis shows that the defect contains metal and suggests that the metal hardmask etch is a contributor. The root cause of such defects, however, often originates from a complex interaction between multiple process steps where the insight and mitigation are closely guarded trade secrets.

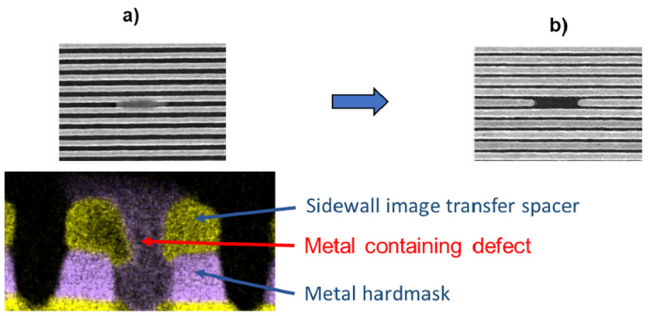

FIG. 13. Top-down and STEM analysis of a defect after SADP pattern assembly in a metal hardmask in (a), and top-down of single line opens defect after Cu planarization (b).

3. Unresolved issues and challenges

Keeping process complexity to a minimum is always preferred in HVM. Pushing the SE EUV limit is, therefore, an attractive option, but it may come with its own set of challenges. Especially when the pitch is decreased to 30 or even 28 nm, there is little or no margin between having resist stringers between resist features versus having resist features that are nearly broken.[40,41] Plasma etching and metallization then results in very low yield, having

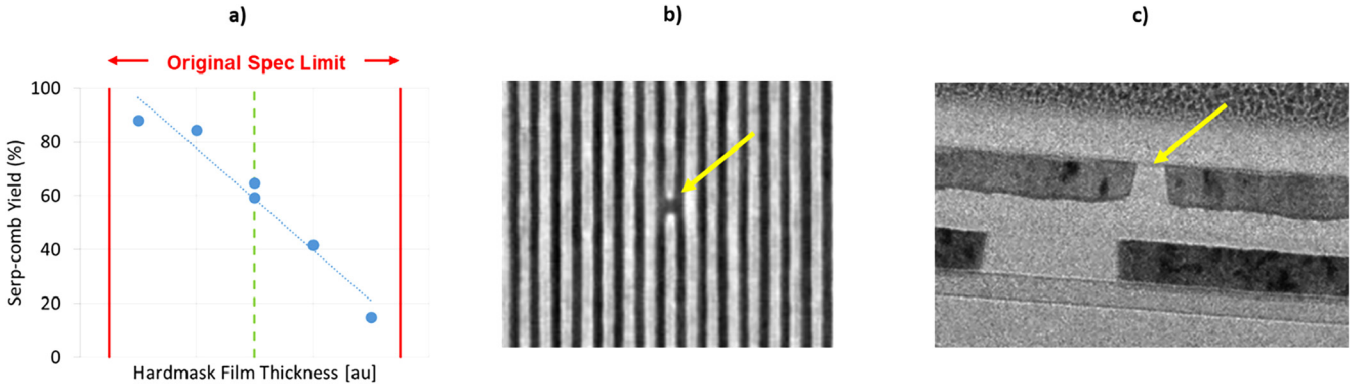

FIG. 12. One-meter-long serp-comb yield for 36 nm interconnect as a function of hardmask thickness in (a) and the corresponding limiting single line opens defect in (b) and (c). The *x* axis in (a) is displayed with arbitrary units to hide the original and confidential engineering specification limits, since they have not been released for publication.

either electrical opens or shorts. One promising approach has been reported by Lutker-Lee[13] and deploys an area selective deposition on the EUV resist in the plasma etch chamber. This patches any broken resist features before the pattern is transferred and improves the process window margin between opens and shorts.

High-numerical-aperture (high-NA) EUV is an exciting new technology entering the early development phase in 2024 with a prospect to extend SE down to a potentially 16 nm pitch. The challenge for plasma etching will be to manage the incoming resist, which must be thinner to accommodate the reduced depth of focus at higher NA. The resist materials will also be an exciting area of co-optimization with plasma etching including metal oxide resists.

The need for plasma etching co-optimization with other processes in HVM applies to all areas of the integration flow, not just BEOL. Plasma etching of the transistor gate is another good and final example where the complexity is akin to Fig. 9(d). With tighter gate pitches and 3D device architectures, such as nanosheets,[42] there are many interdependencies and, hence, a need for co-optimization with etching and process steps across the active area, junctions, replacement metal gate, and even the transistor contacts.

In summary, the field of plasma etching is a very exciting area and critical to getting the next generations of computer chips to market. Addressing these manufacturing challenges requires continued innovation in plasma etching and co-optimization across the integration flow.

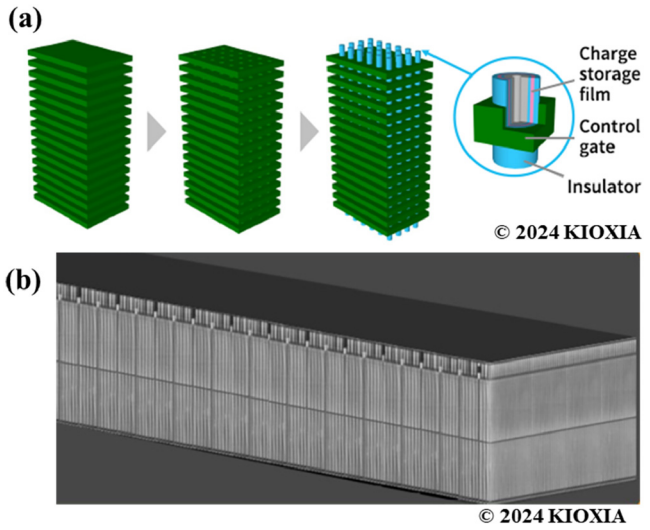

FIG. 14. (a) Memory channel hole etching (punch) and film formation (plug) process for 3D flash memory. (b) Electron microscopy image of BiCS FLASH™ Gen.4. Reproduced with permission of KIOXIA Corporation, https://www.kioxia.com/en-jp/rd/technology/bics-flash.html.

D. High-aspect-ratio processing for insulators and conductors

Kenji Ishikawa, Yoshinobu Ohya, Mitsuhiro Omura

1. Overview

The ever-increasing amount of data handled in the world demands higher performance and integration of semiconductor devices. The scaling-down technologies for 2D integration of devices, such as logic, memory, and sensor, have recently been limited by processing difficulties and device degradation. Therefore, 3D semiconductor devices, such as fin-type field-effect transistors (finFETs) and gate-all-around/nanosheet transistors in logic devices, 3D flash memory devices, CMOS image sensors, and redistribution layers, including through-silicon vias (TSVs) in the heterogeneous integration scheme, have attracted attention.[43] For these, a key technology is achieved by fabricating HAR structures of insulators and conductors (semiconductors).[44] For instance, the processing of deep trench and hole of Si is applied for device isolation and DRAM.[45] The TSV technology is used to stack different types of devices.[46,47] In addition, 3D flash memory has been a pioneer of complicated 3D structure devices as shown in Fig. 14 and one of the most challenging process technologies is memory channel hole etching of SiO/SiN stacked layers. Recently, an innovative etching technique of HAR structures of dielectric films with a hole diameter of approximately 100 nm and 10 μm depth has been reported for 3D flash memory.[11] Plasma etching of HAR insulator structures has been realized by plasma etching systems driven by radio frequencies of several 10–100 MHz to increase plasma density and low frequencies of several 100 kHz to produce high-energy ions perpendicular to the wafer surface for which voltage amplitudes have increased to more than 10 kV.[48] In addition, the high reliability of the equipment is important for high-performance mass production.

This section describes the challenges and future prospects of HAR etching technology for insulators, conductors, and semiconductors.

2. Challenges and roadblocks

Figure 15 shows the challenges of fabricating by plasma etching memory channel holes of 3D flash memory. At the low-aspect-ratio region, there is a strong demand for (i) high mask selectivity and (ii) prevention of critical dimension shifts and clogging. For the medium-aspect-ratio region, (iii) control of bowing and striations should be improved.[49–52] In particular, a deposited film at the HAR sidewall is irradiated with grazing angled ions and a striation pattern can be formed. Once the striation shapes are formed, they can be transferred to dielectric film subsequently.[52] For the high-aspect-ratio region, (iv) the improvement of tapered shape and selectivity over substrate material has been required fundamentally. In addition, the demands on (v) mitigation of HAR shape abnormalities, such as distortion and twisting,[51,53,54] and (vi) control of reactive ion etching (RIE) lag have strongly increased in recent years. The plasma uniformity within the wafer is also becoming increasingly important for 3D flash memory manufacturing. In particular, at the wafer edges, ion tilting impingement toward the wafer surface due to sheath deformation causes misalignment of memory holes as the height of the focus ring decreases by consumption.[55]

For HAR plasma etching systems, ensuring high etch selectivity of insulating materials against carbon-based masks is essential

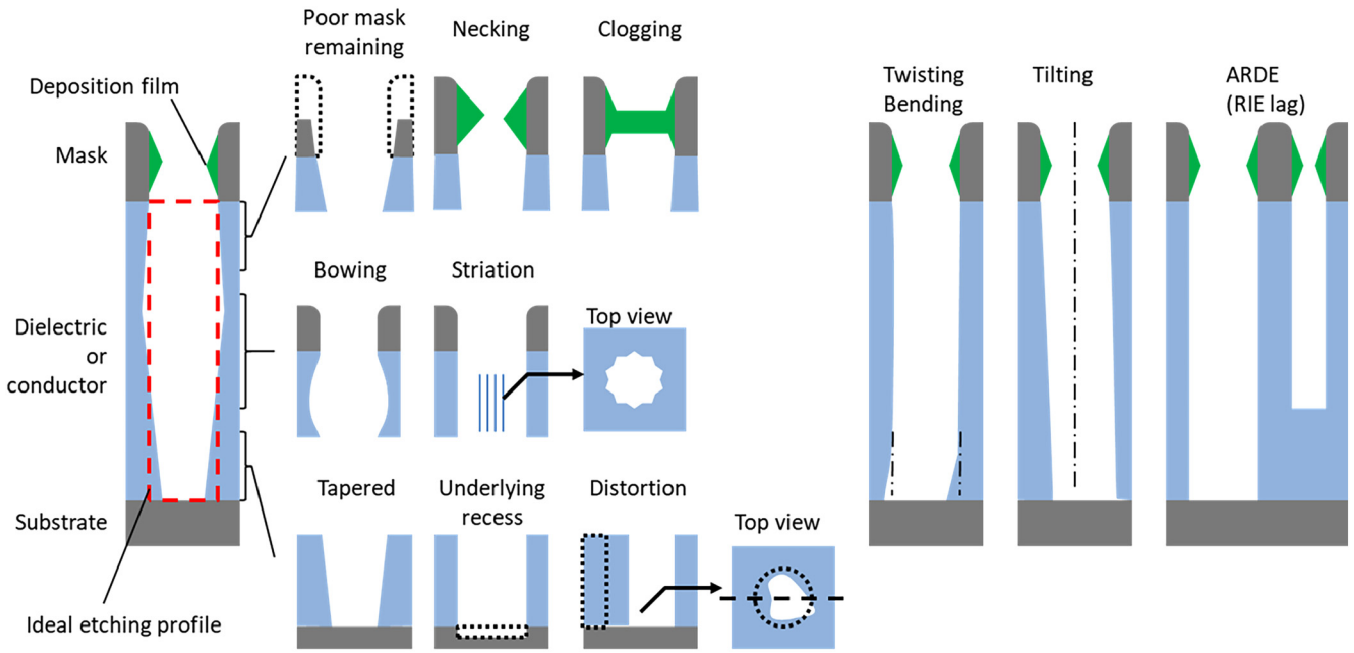

FIG. 15. Issues of high-aspect-ratio features etching in insulators and conductors.

and the use of high molecular fluorocarbons is employed for this.[56,57] At the opening of masks, the heavy fluorocarbons tend to adsorb and deposit, forming a necking shape, as shown in Fig. 15. This necking shape not only inhibits radicals and ions from reaching the bottom but also reflects positive ions at the necking area, inducing a bowing shape. Reducing the bowing effect with respect to adsorption has been obtained by increasing the wafer temperature.[58] A recent innovative approach proposes to use lean gas systems and low substrate temperature to suppress necking shapes while increasing the etching rate of insulating films.[59]

Trade-offs between these issues, such as mask selectivity, clogging, bowing, taper, etc., may be solved by breakthrough technologies, using efficient process optimization methods enhanced by AI/ML techniques.[60] Additionally, overall process optimization in combination with film deposition technologies is actively reported.[59,61] Both of the process and equipment technologies for etching should more aggressively address the shape anomalies, such as distortion and twisting, tilting control, and RIE lag, that are difficult issues to solve by other required processes, such as film deposition technologies. From a device manufacturing point of view, the understanding of RIE lag phenomena will greatly contribute to determining the limitation of processing depth, which is directly related to the device structure.

3. What are the most promising directions for science and technology to overcome the roadblocks?

The question of RIE lag has long been studied for plasma etching processes of various materials including Si, SiO_2, and C. Conventionally, the target dimensions were 1 μm in size and an aspect ratio of approximately 10, but experimental data were limited. For current etch technologies for 3D flash memory, the lateral dimensions have become 10 times smaller, and aspect ratios of 100 in use are 10 times higher than before.[11] Process parameters, e.g., plasma generation conditions, gas chemistry, wafer temperature, etc., are significantly different. We emphasize that for the phenomena observed for HAR etching today, an important question is whether they depend solely on aspect ratio [aspect-ratio-dependent etching (ARDE)], or possibly on feature size.

For HAR etching, eight important limiting factors have previously been discussed.[62] Knudsen transport of neutrals, neutral shadowing, ion shadowing, and differential charging of insulating surface interior of microstructure are particularly important. Dimensional analysis shows that these four mechanisms are consistent with aspect-ratio scaling. For surface diffusion, which is probably important at low temperatures, RIE lag depends on absolute feature size. Other specific mechanisms may be important, e.g., impurities resulting from carbon hardmask interaction with energetic ion bombardment could be a source of carbon for dielectric etching.

For control of ion shadowing, the ion energy distribution function (IEDF) and the ion angular distribution function (IADF) are important to be managed. IEDF and IADF depend on factors such as bias voltage, bias frequency, ion mass, and pressure. Low enough frequency bias with $\tau_{ion}/\tau_{rf} < 1$ can cause a bimodal IEDF, where τ_{ion} is the ion transit time to cross the sheath and τ_{rf} is the rf period. As a result, high-energy ions in the IEDF can be efficiently produced. Although high bias frequency is useful to eliminate large-angle tail of IADF,[63] low bias frequency is effective to accelerate heavier ions.[64] In

the case of HAR insulator etching, low frequency bias has been implemented to accelerate relatively heavy ions for the thick sheath with ~10 kV and to obtain higher maximum ion energy.

To overcome the positive charge-up inside high-aspect-ratio features, which is due to the electron shading effect, it is required to use higher ion energies. Meanwhile, charge neutralization by injecting electrons and negative ions into the high-aspect-ratio feature is desirable. High-energy secondary electrons produced by applying a negative bias voltage to the counter electrode for a pulsed plasma have been used to improve pattern twisting caused by charge-up.[65,66] Moreover, the use of tailored waveforms or DC square waveforms rather than just sinusoidal waveforms is attracting attention for HAR etching applications.[67,68] The inversion of the electric field in the sheath by tailored waveforms and the generation of energetic electrons are recent hot topics.

Importantly, neutral particle transport in HAR structures is key to achieving higher etching rates. Conventionally, plasma etching processes depend on the transport of radicals that easily chemisorb on the HAR sidewalls. The surface diffusion of neutrals at low temperatures should be focused on as a mechanism of RIE lag.[69] The densities of stable neutral molecules for typical plasma conditions are one order higher than that of radicals (species with unpaired electrons). The physisorption of neutrals including multilayer adsorption can be more effective as a transport mechanism for etchants than Knudsen transport, which contributes to etching by ion bombardment at the bottom of the HAR feature. Therefore, the development of approaches that use etching gas chemistry not only with regard to fragmented ions and radical generation via ionization and dissociation but also with regard to the adsorption properties of the gas molecules themselves.

For low-temperature etching processes, control of surface reactions between ions and adsorbed neutrals along with wafer temperature control is essential. For ALE, it has been discussed whether etching is promoted when the physisorbed layer is subjected to ion impact and the possibility that etching is promoted.[70] The etching rate of the silicon dioxide film slows as the deposited fluorocarbon film becomes thicker.[71,72] It is expected that new measurement and analysis techniques will be developed to explore the mechanisms of the reaction layers.[73] The importance of wafer temperature measurement and control is noted.[74] A practical application of excellent measurement techniques has not been achieved yet in high-volume manufacturing.

Sustainability requirements are gaining in importance, including the goal to achieve carbon neutrality by 2050 in the USA. As discussed in Sec. II I, most currently used plasma etching gases need conversion to low global warming potential (GWP) gases.[75] The energy conservation need of semiconductor manufacturing is opposed to the heat input to the wafer by high-power power supplies to control ion energy and incident angle dispersion and wafer cooling technology to promote neutral particle adsorption. New methods for wafer cooling and efficient plasma generation must be developed immediately, so the entire manufacturing process may be optimized.

In HAR processing for device fabrication, the aspect ratio of the etch target continues to change during etching. From the beginning to the last processing, dynamic control of the processing conditions is expected to be the best for ensuring optimal processing condition.[76] Controlling diverse parameters, such as RF system, pressure, gas chemistry, substrate temperature, etc., is difficult, and optimization requires an enormous amount of time and effort. Here, support by AI/ML is expected to improve the efficiency of process development (see also Sec. II O). There are still many issues to be addressed, such as the number and quality of supervised data and handling of sequential reactions. Nevertheless, AI/ML is expected to accelerate future technology development, which is highly desirable.

4. Outlook

For economic and energy-efficient future development of devices, a scientific understanding of the actual process parameters, including ARDE phenomena, and maximum etching rate in HAR processing are essential to understand for determining optimal device structures. For this ion transport in HAR, etching must be revealed in terms of the physicochemical phenomena, including recoil, sputtering, etching in collision with the sidewall surface as a function of ion energy and composition, decomposition of molecules, and charge transfer. Meanwhile, the role of neutral particles must be clarified by understanding transport phenomena including Knudsen diffusion, surface diffusion, and solid or liquid phase. Therefore, as shown in Fig. 16, we need to understand the hierarchically structured kinetics of HAR etching systems in combination with the electrostatic potential distribution, a series of gas and surface reactions, and transport between gas and surface through the boundaries, involving product desorption and evacuation. Both experiments and simulations must be conducted to accelerate research and development.

Plasma generation, gas chemistry, and process control based on these principles are the keys to achieving highly efficient HAR processing. Consideration of the derived mechanism will lead to the creation of HAR etching technology from a broader perspective, including wet etching as well as dry etching.

E. Green chemistry and environmental issues: Precursors and emissions

Nathan Stafford, Jessica C. DeMott, Stephan M. Brandstadter

1. Status and challenges

There are several environmental and health challenges for the semiconductor etching process. Two areas of particular relevance to fluorinated etchants are the carbon footprint derived from the GWPs of these species and the processing of effluent waste streams. Abatement is critical for reducing emissions but is also coupled with needs in wastewater treatment. Here, water treatment considerations related to the topic of per and poly-fluorinated alkyl substances (PFASs) are a developing regulatory area.

The carbon footprint of a typical semiconductor chip manufacturing fab comprises Scope 1, direct emissions, Scope 2, emissions from electricity consumption, including processes that utilize high plasma powers and abatement systems, and Scope 3, upstream and downstream contributors including raw materials, transport and energy efficiency of products and systems.[77–83]

Direct emissions (Scope 1) include contributions from the use of high GWP etchants. The GWP of a molecule is derived from the atmospheric lifetime of the molecule and the wavelengths of light

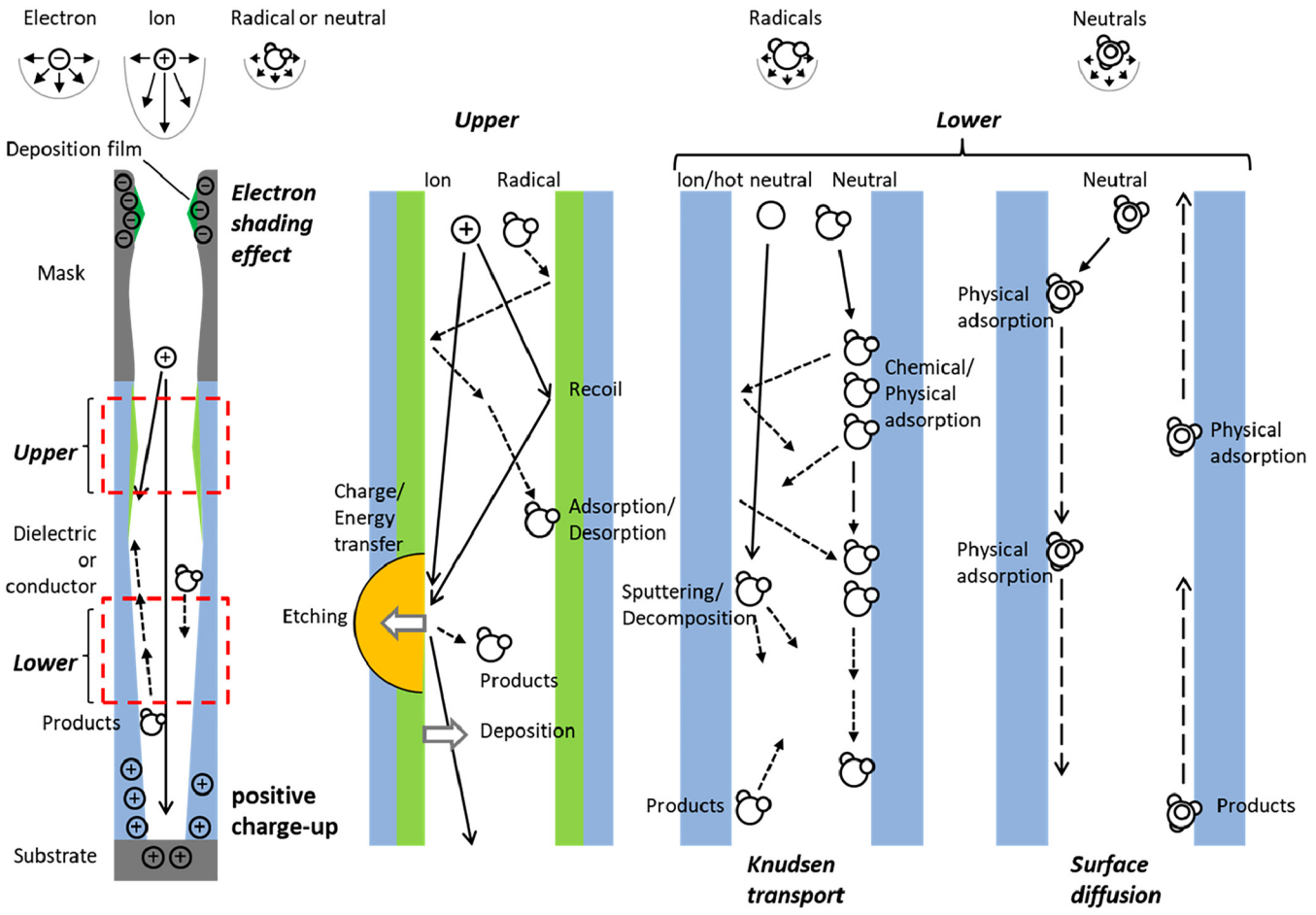

FIG. 16. Key reaction in etching processes of high-aspect-ratio holes and features in insulators and conductors.

the molecule absorbs relative to native atmospheric gases.[84,85] These values are normalized relative to CO_2 and are typically discussed on a 100-year timeframe.[85] Of the etchants, the most impactful to the carbon footprint include fluorocarbons, hydrofluorocarbons, and inorganic fluoride gases. These etchants are used in plasma patterning processes as well as cleaning processes for both etch and deposition chambers. The most common of these are CF_4, C_2F_6, C_3F_8, c-C_4F_8, C_4F_6, C_5F_8, CHF_3, CH_2F_2, CH_3F, and fluorides SF_6 and NF_3. For example, the strong C–F bonds impart stability and increase the molecular lifetime. C–F bonds also absorb energy in spectral ranges where the atmosphere is otherwise transparent (1000–1400 cm^{-1}), contributing to atmospheric heat retention.[84] The same concept applies to SF_6 and NF_3.[86]

According to the World Semiconductor Council, the direct etchant emissions (Scope 1) from semiconductor manufacturing in 2021 was approximately 19 $MMtCO_2eq$ (million metric tons CO_2 equivalent),[87] representing ~0.03% of the world's total CO_2eq emissions.[85] For a given fab manufacturing a 3 nm logic node wafer, lithography and etch contribute 45% of total CO_2 footprint.[88] Process improvements, including abatement technologies, have enabled the semiconductor industry to reduce their direct emissions, normalized to wafer area output, by ~30% since 2010.[87] As can be seen from Fig. 17, NF_3 represents a vast majority of the fluorochemicals used (converted to CO_2eq units[89]). However, thanks to NF_3's high rate of dissociation in the etch process and abatement, the net emissions from NF_3 are less than that of CF_4, which is challenging to dissociate and abate.[90,91]

The nature of the plasma etch process is such that the plasma breaks chemical bonds, forming fragments that can then react with each other and with the wafer, forming new species and eventually exiting the chamber. The etching recipes are often complex, utilizing multiple etchants, inert gases, as well as the addition of oxidizers.[92] Effluent species of some of the standard etching gases have been reported in the literature, including CF_4,[92] c-C_4F_8,[93] CHF_3,[94] and C_4F_6.[95] For c-C_4F_8, the emission species include CF_4, C_2F_4, C_2F_6, COF_2, and SiF_4 in addition to residual c-C_4F_8. In contrast, for the use of C_4F_6, it has been shown[95] that a low GWP gas (C_4F_6) can result in high GWP emission species such as CF_4 and C_2F_6. As

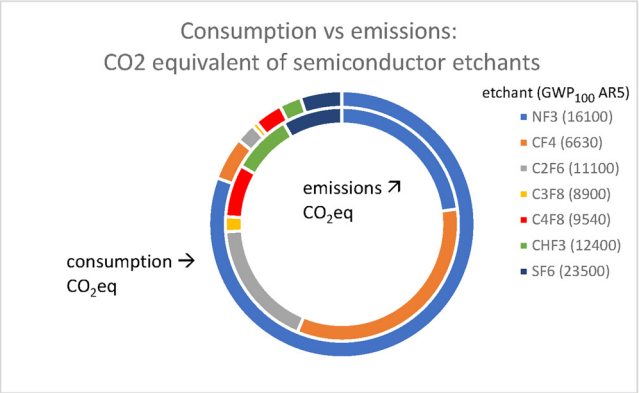

FIG. 17. Comparison of the carbon footprint of PFC/NF_3/SF_6 semiconductor etch and clean gases in 2020 consumed (outer donut) vs emitted (inner donut) as reported by the WSC (Ref. 77) using IPCC AR5 GWP values in parenthesis for each gas (Ref. 89).

such, the emissions from an etching process can be exceedingly different from the incoming gases to the etch chamber often creating high GWP species.

The design of abatement systems must take these complexities into consideration. After exiting the chamber, the effluent is generally treated utilizing several technologies including high temperature combustion, plasma treatment, adsorption, and catalytic based systems. Destruction or removal efficiencies vary based on etchant and abatement technology.[91,93,95,96] For each etchant, the direct emissions impact must account for more than just the GWP and volume of etchant used but also the species generated in plasma and abatement processes.

Fluorinated materials used or created during etch and abatement processes may also be retained in wash streams as trace impurities.[97] Wastewater treatment from the etch process, especially the fluoride content, has been the topic of several papers.[98–101] The current increased interest in PFAS substances, especially as it relates to water quality, is relevant to the use of etchants where highly fluorinated materials are required for silicon etch. The legacy use of the term "PFAS" was to reference long chain fluorinated surfactants, e.g., perfluorooctane sulfonic acid and perfluorooctanoic acid, which have been flagged as substances of concern and have been widely phased out.[102,103] More recently, the use of the term "PFAS" has evolved to include all perfluorinated and partially fluorinated species containing at least a single fully fluorinated carbon. Conflicting definitions continue to evolve from the Environmental Protection Agency (EPA),[104] Organization for Economic Co-operation and Development (OECD),[105] and others;[106,107] thus, the final disposition of this term is still to be determined.

Scope 2 emissions are typically higher for fabs relative to Scope 1 emissions.[80] Key contributions to the electricity demand, and potential areas for Scope 2 reductions, include the use of high-power plasma processes coupled with a number of processing steps, thermal management of equipment, maintenance of cleanroom environments, as well as the energy demand of abatement and water treatment systems.

For upstream Scope 3, the manufacturing, purification, and transport of etchants are considered. Synthesis typically involves the use of fluorine sources such as HF and F_2 generated from inorganic fluoride like fluorspar (CaF_2)[108] and chemical processes that convert organic starting materials to the fluorinated derivatives.[109–111] While publicly available data are limited, the carbon intensity for the production of some fluorinated gases has been reported in the literature.[112–114] Using CH_2F_2 as a representative example, the manufacturing process has reported carbon intensities from 7.77 to 10.9 kg CO_2eq/kg CH_2F_2 produced.[114] It should also be noted that semiconductor manufacturing requires the use of ultrahigh-purity materials, and additional purification steps to deliver electronic grade materials may increase the carbon footprint.[115]

2. Promising developments

There are at least five ways to reduce the overall impact of the etching process: (1) reduce gas consumption (process optimization), (2) change the etchant, (3) reduce power consumption, (4) improve abatement, and (5) reduce process steps. For example, optimization of a CF_4 based spin-on glass etch process as well as the film stack has been demonstrated to result in a drastic reduction of the carbon footprint for both the Scope 1 and Scope 2 emissions of the process.[88]

To address upstream Scope 3 emissions, the carbon footprint of the etch gas supply chain can be improved. Etchant manufacturing improvements can take advantage of synthetic routes that increase product selectivity and reduce the purification burden and associated energy demand. Another consideration can be the use of sustainable raw material feedstocks or waste streams that can be recycled or repurposed. HF, for example, can be manufactured from the H_2SiF_6 produced as a waste stream during phosphate mining.[116]

The need for alternative etchants has inspired a push to develop a stronger understanding of the physical characteristics, process performance, and environmental profiles of fluorinated species.[117] The primary method to reduce the GWP of an etchant is to reduce the lifetime of the molecule in the atmosphere by introducing bonds that are susceptible to temperature, reaction with radicals, and ultraviolet light in the atmosphere. This suggests the inclusion of bonds such as carbon iodine as well as π bonds. For example, the inclusion of one, or more, double bonds is a particularly effective method to increase the reactivity of organic molecules toward OH radicals in the atmosphere.[118] Examples include the cyclic versus double bond isomers of C_3F_6 and C_4F_8, where the GWPs are c-C_3F_6 (GWP = 9200), C_3F_6 (GWP < 1), c-C_4F_8 (GWP = 9540), and C_4F_8 (GWP = 2). Unfortunately, the introduction of a π bond may alter the polymerization of the etchant during the etching process, exemplifying that the direct replacement of high GWP gases with low GWP gases may be very challenging. The substitution of a C–F bond with a C–H bond will also lower the GWP, however to a much lower extent than a π bond. This substitution may also help navigate PFAS considerations. The target is to minimize fluorine content to achieve the required etch performance.

Several new etchants have been reported in the literature over the years with low or lower GWP such as CF_3I,[119–122] C_3F_6,[123–125] C_4F_8,[124] C_3F_6O,[123,125,126] $C_4H_2F_6$,[127,128] C_6F_6,[128,129] $C_3H_2F_4$,[130] fluoroethers,[119,131] and cleaning gases such as F_2[132] and COF_2.[133] Recently, cryogenic etching processes have gained interest especially

in high-aspect-ratio etching and have been reported to reduce significantly the GWP for the process by utilizing HF based chemistry (less C–F chemistry) and increased throughput.[11] The environmental impact of the etching process will remain an important topic in the coming years as the industry implements changes to meet sustainability goals and the regulatory context evolves.

F. Etching of complex materials

Taylor G. Smith, Jane P. Chang

1. Overview

Complex materials based on multielements or multilayers[134] can yield novel and unique properties not attainable with individual constituents and, therefore, are critical in applications such as BEOL interconnects,[135] EUV lithography,[136] topological multiferroics,[137] and spintronics.[138] To realize the desirable device density, these materials typically require patterning that produces vertical sidewalls, causes minimal damage to other devices' structures, and maintains film stoichiometry and functionality.

Patterning complex materials in the gas phase by plasma has been demonstrated by ion-beam etching (IBE), RIE, or ALE. As shown in Fig. 18, a physical IBE relies on an incident ion—usually an inert one such as Ar^+—impinging on the surface with enough energy to "knock off" atoms or molecules from the surface. The sputter yield, as defined by the average number of atoms removed from the target per impinging ion, is a function of ion energy, incidence angle, material composition, and surface temperature. The sputtering yields for single elements can be calculated by literature reported formulation,[141] and the disparity in these yields often causes preferential removal of lighter elements from a compound and a poor selectivity to the mask material. The redeposition of sputtered species within a high-aspect-ratio feature makes it challenging to achieve an anisotropic profile. A plasma-based chemical etching process combines both physical and chemical aspects, where reactive radicals form volatile species on the surface and ions aid in the volatilization of these products.[142] In RIE, these processes occur simultaneously and synergistically. In ALE, these processes are temporally separated, leading to self-limiting surface reactions that remove a single monolayer of atoms at a time.[143] Because volatility of the reaction products is critical in RIE and ALE, the melting points, boiling points, chemical bond strength, and/or vapor pressures of the reaction products dictate the outcome of these processes.

2. State of the art

In this section, patterning metals (which often have involatile reaction products) are used as an example to highlight the current advances. Depending on pattern structure and packing density, metals can be physically sputtered or chemically etched by halogens or organics leading to the formation of metal halides or organometallics. Metals such as W and Ti that form volatile metal halides have been successfully patterned by halogen plasmas,[144,145] with WF_6 having a boiling point of 16.9 °C and $TiCl_4$ of 135.9 °C.[146] Other metals such as Co and Fe can be etched by a sequential plasma etch process where the surface is first chlorinated then

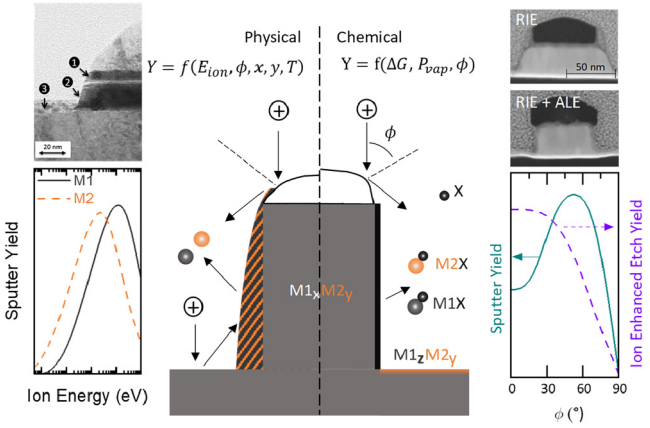

FIG. 18. Patterning of a bimetallic alloy ($M1_xM2_y$) is illustrated for plasma based on (left) a physical and (right) a chemical process (this separation is idealistic, since the physical and chemical components of the etch cannot be completely separated). The sputter yield (Y) of an element is a function of ion energy (E_{ion}), incidence angle (ϕ), material composition (x,y), and surface temperature (T). Physical sputtering leads to sidewall redeposition and hardmask erosion. In a chemically enhanced plasma etching process, the formation and volatilization of the etch products are governed by the Gibbs free energy (ΔG), vapor pressure (P_{vap}), and a distinct ion angular dependence. The preferential removal of one metal over the other as well as the etch selectivity to the surrounding materials are of concern in these patterning processes. TEM images practically demonstrate these principles [Reproduced by permission from Garay *et al.*, ECS Solid State Lett. **4**, P77 (2015). Copyright 2015, IOP Publishing (Ref. 139); and from Xia Sang and Jane P. Chang, J. Vac. Sci. Technol. A **38**, 042604 (2020). Copyright 2020, American Vacuum Society (Ref. 140)].

etched in a hydrogen plasma.[147] Other transition metals form less/nonvolatile metal halides, necessitating alternative etches. In fact, the lack of a viable halogen based plasma etch for Cu, in part, motivated the development of the damascene process for Cu interconnects.[148] Presently, etching Cu has regained interest to form recesses in Cu that prevent overlay error. Hydrogen plasma has been shown feasible in etching Cu in both RIE (Ref. 149) and ALE settings.[150] Additionally, an ALE process using a half-cycle of oxygen plasma and another half-cycle of formic acid vapor has also been demonstrated.[151] Ni has received recent attention due to its use as an absorber layer in EUV lithography. Patterning Ni has been demonstrated by IBE,[152] cyclic H_2/Cl_2 RIE,[140] a thermal ALE process with sulfuryl chloride and trimethylphosphine,[153] and a plasma-thermal ALE process with an oxygen plasma and formic acid vapor.[140,154]

Complex materials involving multimetal elements such as magnetic CoFeB, semiconductor InGaZnO (IGZO), and chalcogenide GeSbTe (GST) are of increasing importance as they allow for precisely tuned properties for various device applications.[138,155] While an IBE process can be used to pattern all these materials, it has a few drawbacks: Sidewall redeposition of sputtered metals can cause shorts in adjacent devices, roughness can degrade the device reliability, and the disparate sputter yields deplete the lighter elements rapidly during the etching process.[156,157]

To mitigate these issues, a chemically based etch process (RIE or ALE) is necessary to pattern these complex materials. For

CoFeB, RIE processes using CO/NH_3 to form volatile metal carbonyls[158] or PF_3 to form metal phosphines[159] have been demonstrated. An RIE process using CH_3COOH/Ar has also been shown to etch CoFeB as well as the other materials in a magnetic tunneling junction stack, but because of the Ar^+ ions, the process had poor selectivity to the W/TiN hardmask.[139] ALE processes using a solid state electrochemical cell to chlorinate the surface followed by exposure to acetylacetonate (Hacac) has shown improved compositional control and reduced Gilbert dampening.[156] A detailed review is available on etching CoFeB and other magnetic materials.[160] For IGZO, both RIE and ALE have been demonstrated;[161] however, both left the feature sidewalls enriched in Ga, shown in Fig. 19(a). Field-effect mobility and threshold voltage of IGZO thin-film transistors have been shown to be highly dependent on the stoichiometry of the IGZO layer, necessitating tight compositional control.[163] For GST, many etch chemistries are discussed in a recent review.[162] While halogen plasma chemistries are effective in patterning GST, undesirable residues formed when a halogenated surface is exposed to atmosphere.[164] Another complication of GST is that Ge tends to segregate from the surface post etching, forming GeO_x after even short ambient exposures.[164] The formation of nonstoichiometric surface layers negatively impacts the recrystallization of the GST, an effect worsened by halogens [Fig. 19(b)].[165] It was found that a halogen-free Ar/CH_4 plasma process effectively etched GST while still maintaining an appropriate crystallization temperature.[162]

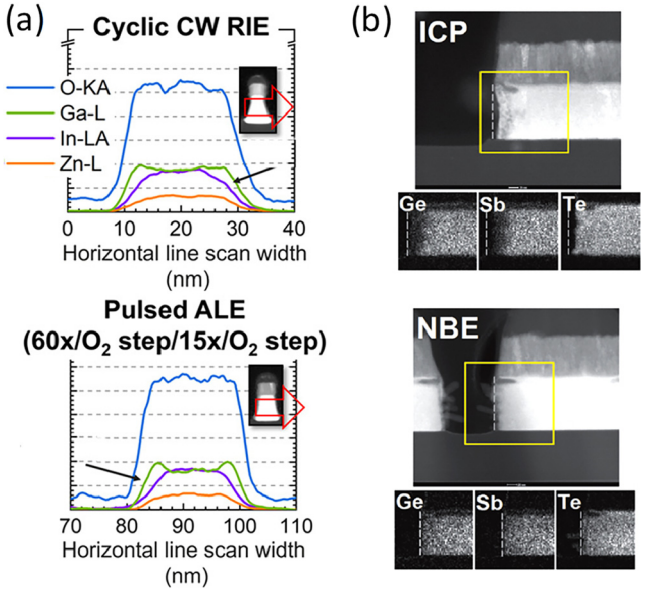

FIG. 19. (a) Elemental linescans of IGZO films patterned by cyclic CW RIE and pulsed ALE processes—both led to Ga enrichment at the sidewalls. (b) EDX image of the etched sidewall of GST, showing Ge and Sb depletion from an ICP plasma, which can be mitigated in a neutral beam. Reprinted with permission from Kundu *et al.*, ACS Appl. Mater. Interfaces **14**, 34029–34039 (2022). Copyright 2022, American Chemical Society (Ref. 161); and from Shen *et al.*, J. Vac. Sci. Technol. A **38**, 060802 (2020). Copyright 2020, American Vacuum Society (Ref. 162).

3. Unresolved issues and challenges

There are many issues inherent to patterning complex materials. For a physically based etching process, differing sputter yields lead to preferential physical removal of some elements over others. This effect, though it can be minimized by tuning ion energies, incidence angle, and other process parameters, cannot be completely eliminated. Additionally, sidewall redeposition, although mitigated by tilting the sample during etching, remains an issue since the sputtered species are not inherently volatile. Although recent work has capitalized on redeposition to create peculiar features of Pt, Ti, and Si,[166] in general redeposition leads to tapered sidewalls and shorts between vertically aligned elements. Chemical etching also has inherent limitations due to the product involatility. Metal halides, hydrides, and other complexes have different volatilities depending on the central cation, resulting in preferential etching of certain elements. Volatility diagrams can be constructed based on available enthalpies, entropies, and activity coefficients from databases such as the National Institute of Standards and Technology-Joint Army Navy Air Force (NIST JANAF) tables to aid the screening of viable chemistry/mixture that volatilizes all elements in a film.[147,167] Density-functional theory (DFT) and other simulations can also be used to theoretically assess the viability of potential etch processes before costly experimental verification is undertaken.[168]

Etching complex materials is also complicated by integration with other structures, hardmasks, and features. An etch chemistry must selectively etch the target material and not the hardmask/photoresist (see Sec. II B), underlayers, or other exposed features. A physical based plasma etch process often removes materials indiscriminately, while a chemical process requires a careful selection of etchants in order to achieve selectivity. AR dependent etching, as discussed in Sec. II H, is another issue for many plasma processes, where features with larger critical dimensions etch more quickly than smaller ones.

To mitigate the challenges of etching complex materials, tailored approaches are necessary. Leveraging the fact that plasmas can both etch and deposit materials, a balance between these two processes can potentially minimize sidewall damage.[169] Etches can also be cycled to maintain stoichiometric control. For example, if an etch process selectively removes M1 over M2 (as shown in Fig. 18), it can be cycled with another process that preferentially removes M2.[170] These cycles can consist of complementary IBE, RIE, and/or ALE processes. Finally, ALE promises improved compositional control for many of the materials discussed here, and recent advances in ALE equipment have significantly increased its throughput, making it viable in supporting high-volume manufacturing[143]—see also Sec. II M.

G. Future of plasma etching for microelectronics—Applied Materials perspective

Shahid Rauf, John Poulose

1. Overview

Plasma etching is a critical technology for the fabrication of microelectronic circuits. Since its early days in the 1970s, plasma

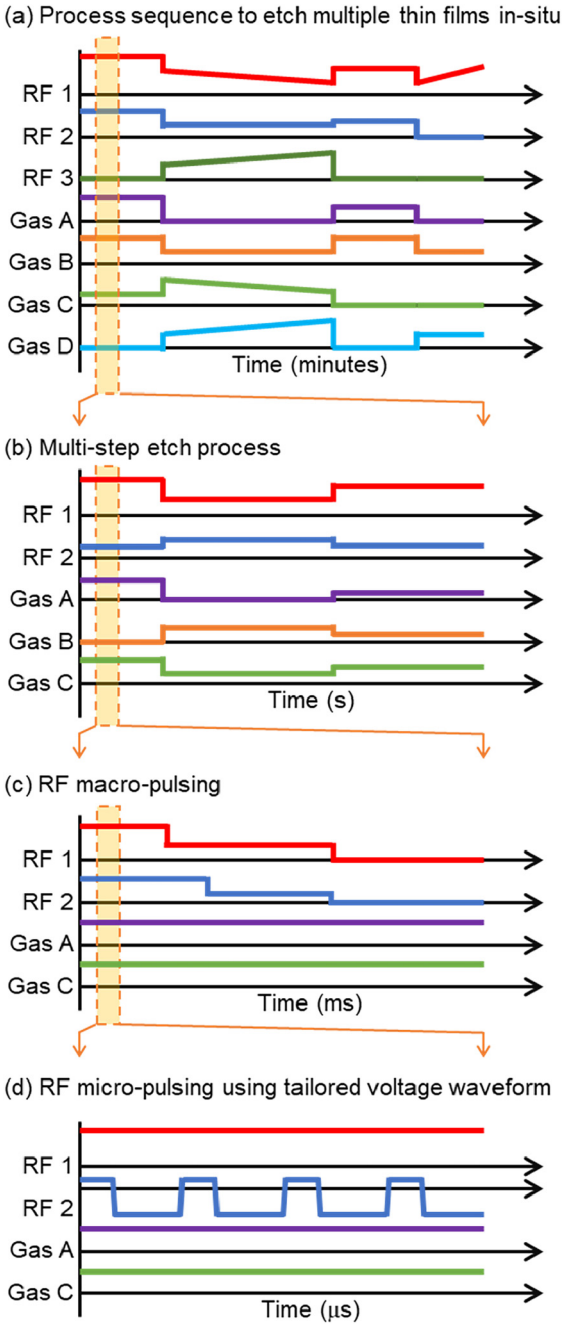

FIG. 20. Anatomy of a typical etch process sequence. (a) Multiple thin-film layers are etched *in situ* using a sequence of etch processes, each requiring different chemistries and conditions. Some control parameters might be ramped during the process. (b) Each etch process can include multiple steps with rapid transitions between the steps to accurately control conditions on the structure bottom and sidewalls, and the mask. (c) RF power or voltage during the steps is usually pulsed on ms timescale to control the IAEDF and neutral/ion ratio. (d) One can control the IAED and neutral/ion ratio further using tailored voltage waveform for bias.

etching systems have been continuously improved and it's possible today to economically fabricate devices and structures with a few nm critical dimensions. Such feats of engineering are, however, only feasible using highly complex etching processes. As illustrated in Fig. 20, a typical etch recipe in the semiconductor industry can have 10 s of steps, many of which would involve pulsing of multiple RF sources and repeated transition from one complex chemistry to another. The goal is to control the plasma-surface interaction processes on the patterned wafer surface on a nm spatial and μs time scale. The limits of plasma etching in HVM would be dictated not only by what is technically possible but also by our ability to manage the complexity of etch processes economically. In our opinion, the future of plasma etching hinges on how well we understand the dynamics of plasma-surface interaction processes on a nm and μs scale, how precisely we can control these surface processes, and how we make better use of real-time information available on plasma etching equipment to enable such control.

2. Promising options

Among the many methods used to control the dynamics of plasma etching processes, RF pulsing[33] has proven to be one of the most important. Multiple RF sources are used on modern etch equipment to generate the plasma and control the electron and ion characteristics. By pulsing these RF sources between different levels (including turning them off), it is possible to quickly transition between different etching and deposition regimes. RF pulsing allows one to tailor the ion energy and angular distribution function (IAEDF) as well as the neutral/ion flux on the wafer surface on a ms timescale. Tailored voltage waveform[171] enables the control of these properties including the IAEDF on an even faster timescale. By changing the etching gases between etch steps, as done in atomic layer etch,[172] one can control the plasma properties even further, albeit on a slower timescale. The complexity of a typical etch process in HVM is illustrated in Fig. 20. With multiple RF power supplies and gases available on modern plasma etching equipment, it is possible to design an infinite number of pulsing schemes with minute control over the etch characteristics. Such engineering hinges on our understanding of the dynamics of plasma-surface interaction processes deep within high-aspect-ratio features, which is rudimentary at best even for simplified process controls. Pulsing of multiple RF sources requires fast closed-loop control of an increased number of control parameters. The RF system also needs to be able to handle the frequent transition between plasmas with significantly different impedances. A major challenge is that the plasma dynamics become increasingly complex due to cross-interactions when multiple RF sources are pulsed.

Due to our relatively crude fundamental understanding of plasma-surface processes within features, most plasma etch process development is done using trial-and-error experimentation. With little real-time insight into the dynamics of the etching process, the process engineers typically rely on postetch microscopic and surface analysis data. This is supplemented with basic physics and chemistry know-how, but such knowledge is generally only available for simple situations or planar films. Dynamic information about the etch process is usually only available from indirect sensors such as optical emission spectroscopy (OES). The etching

of 3D structures relies on the careful balance between many fundamental processes on the surface in contact with the ions, radicals, electrons, and photons from the plasma. These processes include chemisorption, physisorption, sputtering, reactive ion etch, sputtering, chemical etching, surface diffusion, and bulk diffusion. As plasma etching is usually done within narrow structures involving multiple materials, different portions of the surface experience a different mix of species from the plasma and different combinations of these fundamental surface processes. The dynamics of these processes on important materials and chemistries as well as charged and neutral species transport within narrow structures need to be better understood. Wafer temperature, both cryogenic[173] (<0 °C) and hundreds of °C, has proven to be an important parameter for controlling the etching characteristics. Our understanding of plasma-surface interaction processes at low temperatures needs refinement. In addition, the semiconductor industry is always seeking new chemistries that provide better control of etching and deposition within features.

Due to the complexity of the plasma-surface interaction processes and uncertainty about the dynamics of what happens within narrow features during etching, models for plasma etching are not at the stage where they can be used to design etching processes without significant experimentally guided model tweaking. The most widely used methods start with an assumed plasma-surface interaction mechanism with many free parameters and evolve the surface by either solving differential equations[174] or particle-based Monte Carlo techniques.[175] The free parameters are ideally adjusted using model-experiment comparison over a wide parameter range. However, experiments are expensive and there can be many free parameters in the model. The etch mechanisms are, therefore, not unique or necessarily valid outside the parameter range of validation. These models do allow simulation of etching within 3D structures and exploration of the underlying physics and chemistry, but they lack predictability. Next in complexity are molecular dynamics (MD) models of plasma-surface interaction.[176] The MD models are more fundamentals-based but they need to be more thoroughly tested against experiments and are limited to small domains due to their computational expense. The MD models of plasma etching need to be expanded to a larger range of materials and species and used to model patterned surfaces. Fundamental quantum chemistry methods[177] are currently limited to structures with a small number of atoms and are typically only used to examine chemical processes on surfaces without energetic ions or electrons.

As the environment within a plasma etch reactor is harsh and one needs to strictly control contaminants, the range of real-time sensors that can be used in etching chambers is limited. Most sensors are external, such as OES and RF measurements. These sensors, in principle, contain valuable real-time information about the plasma and dynamics on the wafer surface undergoing etching. However, data from these sensors are indirectly linked to the surface processes, and extracting valuable etch-relevant information from this data is nontrivial. The uses of OES for end-point detection and RF for impedance matching are well-established, but it is valuable to understand what more can be learned about real-time changes on the surfaces using production-compatible sensors. Improved sensor capabilities add additional data streams that must be calibrated and monitored, in some cases doubling from previous generations. The growth of data available on etch tools is illustrated in Fig. 21.

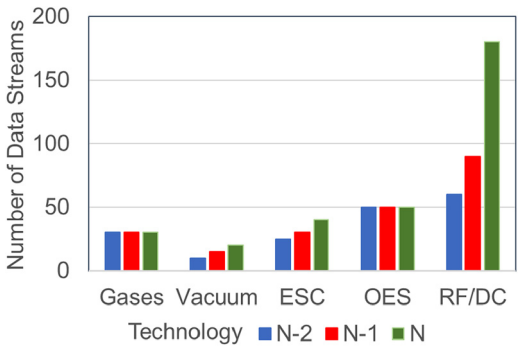

FIG. 21. Number of data streams available on etch tools is increasing rapidly as the etch processes become more complex.

The generic promise of AI based tools exists but lacks the mechanistic understanding of plasma-surface dynamics, which is correlated to sensor outputs. Can alternative AI methods be used in this development?

The need for alternative sensor development and analysis, instead of additional sensors, could help reduce the complexity by providing simpler ways to characterize the plasma interactions. Three-dimensional diagnostics of transitory bulk plasma states[178] have provided useful insights into the plasma dynamics in pulsed plasmas. HVM-compatible diagnostics that provide similar information for real-time control are lacking but would be useful. The need for model based predictive algorithms would be important to close the bridge between control systems that exceed closed-loop response and require the use of open loop systems that can preemptively transition the plasma state.

The harsh environment in plasma etching reactors makes the selection of plasma-facing materials and coatings critical. These surfaces act as a reservoir of etching and depositing species and can also be a source of contamination. Careful management of these surfaces is critical for advanced etching applications, where specs for defects and run-to-run variability are tight. Progress continues to be made to develop new materials and coatings for plasma etching chambers, especially for logic applications where defectivity management is critical.

With the prevalence of 3D devices and ever-shrinking CDs, it has become increasingly difficult to supply energetic ions and neutral radicals to the etch front within features. The primary means of retaining productivity is to increase the RF powers, thus generating a higher plasma density with more energetic ions. This trend is, however, not sustainable. It is important to carefully examine how power is used in plasma etching reactors and how to improve the efficiency of etch processes. The move toward cryogenic etching[173] is further increasing the energy demand. Some of the efficiency improvement would come from optimizing the etch processes and migrating to gases that allow more efficient etching. However, research into better RF amplifier designs would also help. Increasing the RF pulsing complexity generally requires the use of more dynamic power amplifiers, which are usually less power

efficient with upward of 20% points efficiency decrease, hampering conflicting green initiatives. Etching has traditionally relied on many gases with high GWP. As described in Sec. II J, it is important to explore alternative gases that have lower GWP.

As device dimensions and critical film thickness approach the nm range, damage caused by ions in commonly used RF plasma sources, even without external bias, becomes a limiting factor in many applications. It is, therefore, useful to examine plasma sources, such as electron beam-generated plasmas,[179] where ion energy is lower. Etch processes that rely on only radicals, for example, those obtained from remote plasma sources, can provide high selectivity and are of interest. In addition, alternate means of energy delivery for etching, such as using electrons[180] and photons,[181] should be explored.

H. Future of plasma etching for microelectronics—Lam Research Corporation perspective

Richard A. Gottscho, Keren J. Kanarik

1. Overview

The strategic importance and economic value of semiconductor technology, including high-volume manufacturing, is widely recognized.[182] The key to competitive high-volume semiconductor manufacturing is process equipment machinery. Etching is on the critical path to new technology enablement as much as is lithography, the traditional technical driver of Moore's law.[183] Etching and deposition have enabled patterning beyond the wavelength limitation of lithography through shrinks, double patterning, high-aspect-ratio etching and filling, and gate-all-around formation.

2. Challenges and roadblocks

Certain challenges in etching have not changed for the last 40 years: selectivity, profile control, wafer-scale uniformity, feature-scale uniformity, throughput, defectivity, and overall cost of ownership (CoO). What has changed are the solutions to those challenges as device dimensions, materials, and structures have all evolved (Fig. 22). Atomic-scale precision on both the feature-scale and the wafer-scale is now required. The number of steps to make a device continues to grow with each new node.[184] With this increased complexity, time to solution and cost of the solution has also increased. None of these are good trends. Additional requirements for environmentally sustainable solutions make the challenges even more formidable.

For selectivity, the good news is that ALE and ALD have matured to the point where they have been adopted in high-volume manufacturing.[31] With self-limiting reactions, very high selectivity is achievable, in principle. However, to reach that limit, compromises in throughput and, therefore, CoO have been required. Another challenge in ALE is controlling the flux of reactive species from the walls of the reactor: even if the reactor is evacuated after each surface modification step, residual gases desorbing from walls result in adventitious etching and loss of self-limiting behavior and selectivity. Imprecise ion energy control can also result in reduced selectivity and increased surface roughness. More research into atomic layer etching is needed. Can we find better material systems for self-limiting reactions? Can we find better solutions for managing reactor wall contamination and outgassing? What can be done to reduce ALE cycle times? Can smaller volumes and higher flows provide higher throughput without inducing larger wafer-scale nonuniformities?

Profile control remains a persistent challenge but is particularly difficult for high-aspect-ratio structures. In 3D NAND, aspect

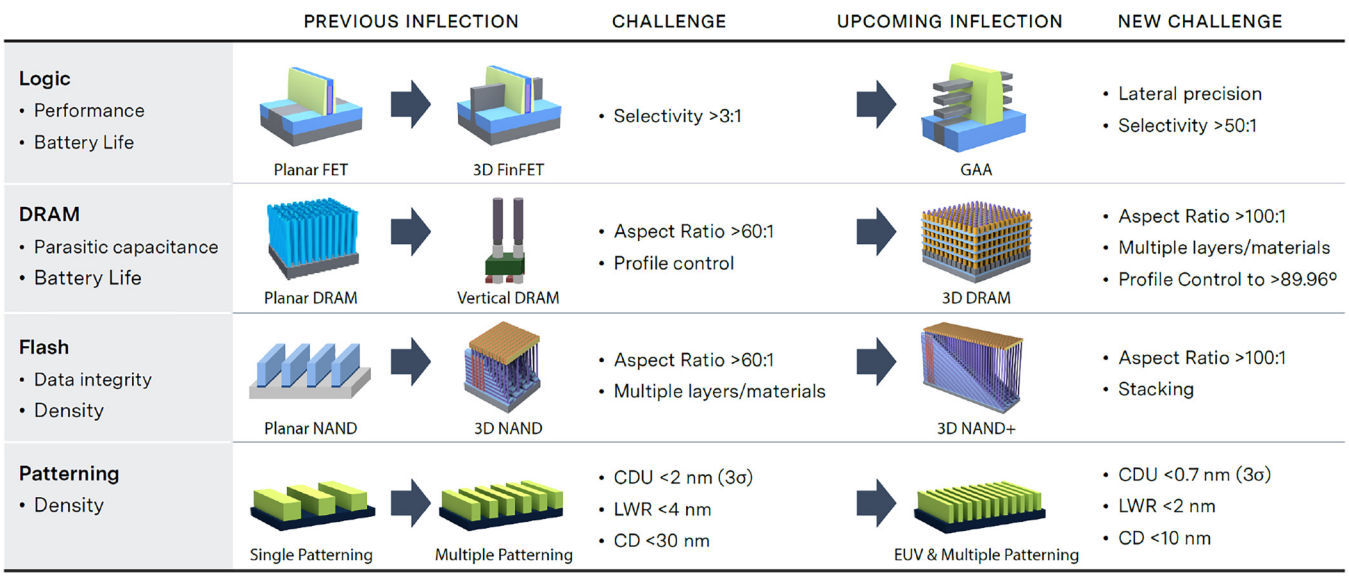

FIG. 22. Technology trends and challenges in etch, comparing ten years ago to today.

ratios are approaching 100:1. To address high aspect ratios, the industry implemented pulsed plasma processing to obtain better control of the ion energy and angular distributions. Pulsing enables independent control of ion and neutral flux, which helps with selectivity as well as profile control.[185] Higher voltages have been another trend and can be expected to continue, but this trend only aggravates the energy intensity of plasma etching. As outlined initially by Wang and Wendt,[186] the applied waveform can be tailored both to sharpen and tune the ion energy distribution function. This technology is only now coming to fruition. Concomitant with waveform shaping and higher voltages is the reintroduction of low-temperature etching whose use can simplify the chemistry while introducing new mechanisms for reactant transport into high-aspect-ratio features.[187] The engineering challenges of low-temperature processing with waveform shaping and high voltages cannot be underestimated. More basic research into mechanisms and chemistries is also needed. Now, with the advent of gate all-around (GAA) structures, we are presented with a new set of challenges in what we call "perpendicular" etching, where etching occurs downward and then at right angles to the left and right, as shown in Fig. 23. How is dimensional control achieved with high selectivity when etching is perpendicular, without the synergistic benefits of ion bombardment? Even with new chemistries that are inherently selective, without ion bombardment, how will the industry deal with the challenge of removing surface contamination that can result in blocked etch defects?

For feature-scale uniformity, the advent of pulsed plasma processing and the control of ion/neutral flux ratio during an etch have proven invaluable. With atomic layer and low-temperature etching, the limits of aspect-ratio-dependent etching have been consistently extended and process windows have expanded even as requirements have grown more stringent. For wafer-scale uniformity, however, the industry has long struggled with the edge problem: finite wafer size induces discontinuities not only in electrical potential but also chemical potential at the wafer edge.[188,189] The strategies to deal with this problem always entail trade-offs because each species exhibits a different response to the discontinuities. Solutions also entail adverse cost impact: for example, to maintain precise control to 2 mm edge exclusion, edge rings are replaced often. Powered and temperature-controlled edge rings offer superior control and longer times between part replacements but entail higher cost. The advent of self-maintained machines, where edge rings are replaced undervacuum robotically, offers a respite to the trend of ever-increasing product cost.[190]

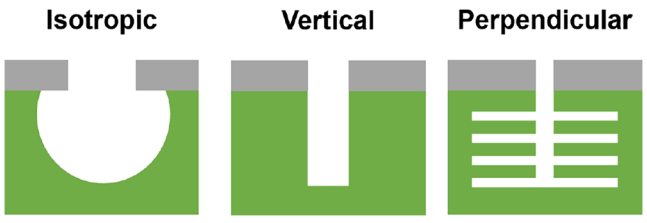

FIG. 23. Schematic of "perpendicular" etching (relative to isotropic and vertical etching), which is needed to produce 3D structures, such as GAA.

3. Outlook

Given trends in device technology—atomic-scale precision, 3D architectures, complex device structures—dramatic improvement in productivity for the fabs is needed. While it is tempting to think that larger wafer size would solve this problem, the vain attempt to move the industry to 450 from 300 mm showed that such a solution path was not promising. Instead, the industry must move to equipment sets that are self-aware, self-maintained, and self-adaptive. The fabs of the future will be "lights out" with unprecedented tool reliability. Robots will perform routine maintenance and thereby reduce variability and provide a more reliable return of tools to production. Much work is required to transform today's equipment sets to those that can be fully maintained robotically.

To deal with these challenges, the more stringent requirements, and greater complexity in a world where the pace of innovation is accelerating, a new paradigm in R&D is required. R&D normally starts by testing small coupons approximately 1/50th of a whole wafer in reactors ~1/10th the size of production tools. Such miniaturization allows >10× experimental cost reduction and higher flexibility by using interchangeable parts for chemical delivery, hardware, software, controls, and materials. However, scaling results from such systems to high-volume manufacturing systems is not well understood and, therefore, not easily accomplished. In practice, it can take more than a year to translate results from one chip to a full wafer for the most challenging applications. Then, the results must be scaled again from one wafer to many wafers and from one chamber to many chambers.

Why does it take so long and cost so much money for a learning cycle? This cycle consists of formulating a hypothesis, designing an experiment to test the hypothesis, executing the experiment, and analyzing the results. The bottleneck in etching and deposition processes is often metrology based on electron microscopy, which is destructive, expensive, and time-consuming. For most etch process development, it is necessary to run a series of partial etches to understand profile evolution, further increasing the number of images required for one process condition. Engineers often do not see the results of their experiments until the next day. What is more, these engineers typically run batches of four to ten experiments to make use of limited tool time and compensate for slow metrology turn-around. Even if one of those experiments pays off, the net result is higher cost and higher waste.

Instead, imagine we had a metrology with atomic-scale resolution that enables us to measure—in real time—the evolution of the profile (not just depth) of a sub-10 nm hole or trench as it is being etched or filled.[191] Cycles of learning would be dramatically reduced, as would the number of experiments required to reach a solution. Engineers would be able to watch the results of process changes as they occur. We estimate real-time metrology could provide >100× reduction in experimental costs and time.

Even with real-time metrology and other cost-reducing innovations, physical laboratories will always be expensive. It is important to leverage those expensive investments in physical assets by capturing and curating the data generated while developing reactors and the processes that run in them. These data can then be used to calibrate hybrid physics-data-based models that, in turn, can be used to find and/or extend the process window and scale from

small-to-large at a fraction of the cost and time compared to physical experimentation.[192,193]

Similar approaches can be applied to every aspect of development up and down the technology stack. Imagine every tool, every process, and every integration having a virtual representation that is more accessible than the network of physical assets alone. Such virtualization can enable crowd-sourced solutions. To build better models, we need more fundamental data on the interactions of reactive species—charged and uncharged—with material surfaces and with each other in the plasma environment. We need to study and understand mechanisms for transport and reaction on surfaces over wider ranges of temperatures and other process conditions.

The virtual environment can also serve as an inexpensive and safe training ground, where less promising ideas can be eliminated prior to experimentation in the real world, thereby making the productivity of our laboratories and pilot lines greater. Note that advances in experimental methods, such as real-time metrology, only enhance the pace of new data generation and the maturation of this virtual laboratory. We estimate the potential cost savings of this approach to be substantial. Of course, real experiments in the physical laboratory remain vital as they constitute ground truth. We aspire to using fewer real experiments for the same output, using fewer resources, thereby cutting costs and time while promoting sustainability.

I. Future of plasma etching for microelectronics—Tokyo Electron Limited perspective

Pingshan Luan, Peter L. G. Ventzek, Akiteru Ko

The continuous scaling of CMOS feature size on silicon has been the steady driving force for generations of wafer processing equipment (WPE) and numerous process innovations. The role of WPE vendors in the microelectronic industry has been to enable scaling with the highest performance at minimum cost. As we stand in the post-Dennard scaling[3] era, severe challenges arise and imperil many conventional plasma-based processes. The demand for "fab-ready" technology breakthroughs is unprecedented.[194]

1. Challenges of industrial plasma etch are moving targets

A successful industrial etch application often emerges at the right time for addressing the right scaling challenge using sometimes existing concepts. WPE vendors initiate tool development cycle 2 technology nodes ahead of the current production node, often starting from improving upon proven successful chambers. Although the principles applied are universal, the plasma etch challenges are moving "targets," which change from node to node. It is crucial for WPE vendors to understand, meet, and predict the hardware and process demands of future nodes charted by the integrated device manufacturers and fabrication plants (Foundries). Sometimes an etch concept might be ahead of its time, and at other times an "obsolete" idea might make a comeback for new applications. It is the constant creation and accumulation of etch-related technologies that enable WPE vendors to address evolving demands.

One example of such a development cycle is the application of magnetically enhanced plasma in dielectric etch. The idea of magnetron plasma dates back to 1939;[195] however, it is not until the late 1980s when magnetically enhanced RIE (MERIE) became appealing to etch applications.[196] This is due to its ability in generating high plasma density without excessive bias voltage, thus offering high etch rate (ER) and low material damage.[197] The high etch rate of MERIE, often in micrometers per minute (μm/min), was desired for throughput when the critical dimensions were in the μm to sub-μm range. To mitigate magnetically induced drifts, industrial MERIE tools were designed with oscillatory magnetic fields, such as rotating magnets on Tokyo Electron's Dynamic Resource Management (TEL DRM) chamber.[198] In the past decade or so, MERIE has faded away, mostly because the shrink of CD renders μm/min ER unnecessary. However, an external magnetic field brings one more degree of freedom into controlling the plasma, and this concept could be "recycled" and reapplied for uniformity and profile control in future applications.

The challenges in industrial plasma etch originate from scaling (see Fig. 24). First, for X-Y (planar) scaling, plasma-based patterning development is dominated by the adoption of extreme ultraviolet (EUV) lithography and overlays.[199] It has been reported there is a triangular trade-off relationship among resolution, exposure dose, and defect control in EUV lithography.[200] One of the three must be sacrificed if the other two are defined. Due to the optical constraint of EUV lithography and low dose requirement for throughput, plasma etch is asked to mitigate defects originating from EUV patterning, such as LER and stochastics-printing errors (scum, breakage).[201,202] Promising technology includes resist hardening by energetic or reactive species from plasma,[203] printing error repair by plasma-based deposition-trimming cycles,[204] and direct scum removal using energetic species.[201] Furthermore, the recent progress on metal compound EUV photoresists,[205] with their promising improvement on sensitivity and resolution, also demands for innovative plasma etch processes.[206] Second, for Z (vertical) scaling, the arrival of 3D device architectures requires etch chambers to address transport issues intrinsic to HAR structures.[44] For example, in 3D-NAND memory applications, conventional etch processes are often limited by low ERs in the HAR region.[59] A paradigm shift in the etch process that allows high ER at HAR region without sacrificing profile is desired. So far, plasma etch at cryogenic temperatures has shown great promise, as demonstrated by Kihara *et al.*[11] on 300 mm production tools. Last, at the architecture level, the 3D heterogeneous integration of processors, memories, and other integrated circuits[207] demands for innovations in TSV/through-dielectric via etch and plasma-activated surface bonding processes.[208]

2. Challenges in mechanistic understanding of plasmas and surfaces

Controlling and optimizing plasma etch processes requires an understanding of both the plasma and material surface. Plasma etch processes are essentially surface phenomena that involve the multicomponent mixture of neutrals, electrons, ions, and photons from plasma. Unfortunately, there are no such physical knobs as "ER," "selectivity," or "uniformity" on production tools. It is rather the users who must convert these process metrics on silicon into

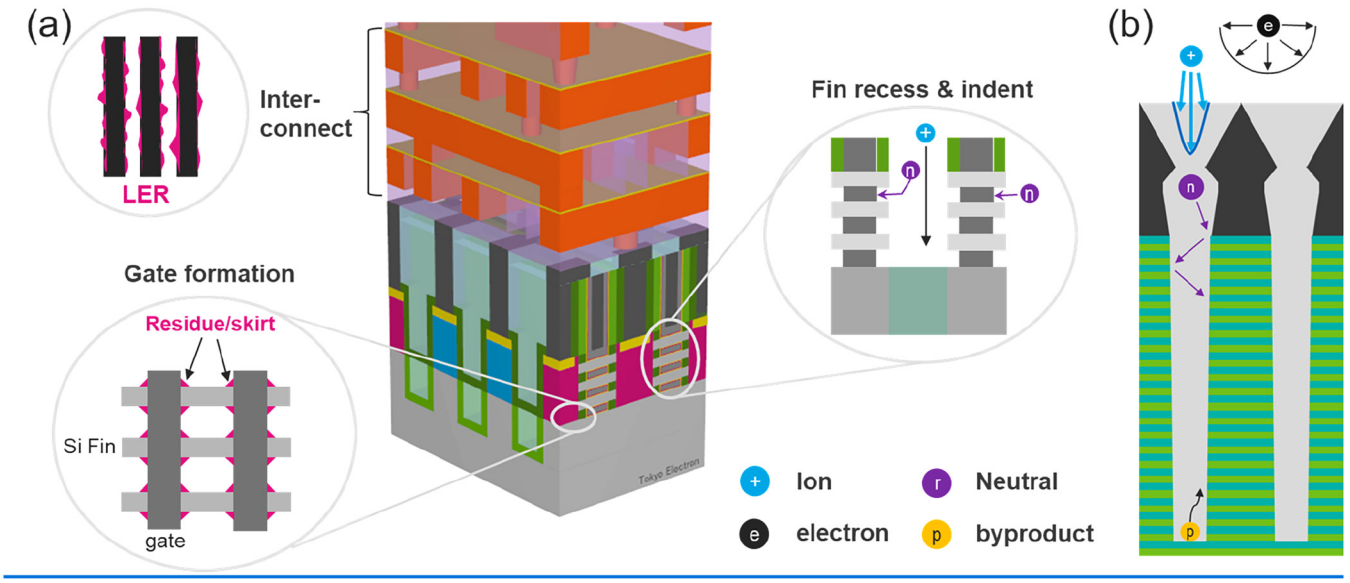

FIG. 24. Examples of plasma etch challenges in (a) logic GAA transistor and (b) memory 3D-NAND applications. During GAA transistor formation, etch processes are asked to fabricate both vertical and horizontal structures with ultrahigh selectivity, directionality, and profile integrity. Residues and surface roughness at the corners of features in sub-10 nm scale need to be minimized. During metal line formation, line-edge roughness (LER) control is critical. For memory applications, the challenges of plasma etch come from the transport of various species in HAR features including ions (+), neutrals (n), etch byproduct (p), and electrons (e).

tool input variables such as power, pressure, flow rates, etc. This conversion has never been straightforward as the type, dose, and energy of various species delivered from plasma are often entangled.[209] Analytical models for simple chemistry in parallel plate configurations do exist,[210–212] but their predictive accuracy diminishes when applied to complex geometry and reactive gas environments. The lack of sufficient chemical reaction databases for the gas (plasma) phase and surfaces also makes numerical modeling challenging.[194] Often, process engineers revert to empirical methods and intuition for process optimization.[213] With the increasing degree of hardware sophistication and the atomic level process tolerance, it is unsustainable to brute force development through permutations of tool parameters.[193]

Advanced diagnostics provide not only essential data for the mechanistic understanding of plasmas and surfaces but also means for production monitoring and control. First, at the equipment design level, diagnostics are needed for understanding the generation and characteristics of plasmas. Good chamber designs should offer the control of plasma properties through decoupled input variables. One such example is inductively coupled plasma (ICP) with capacitively coupling—to a certain extent the source power controls ion flux whereas the bias power controls ion energy.[214] Diagnostics serve the crucial role of providing experimental data and the validation of modeling, especially for novel plasma generation regimes such as advanced pulsing[185] and nonsinusoidal waveforms.[215,216] It is important to measure the density of electrons and ions, electron energy distribution function, time resolved ion energy and angle distribution function on wafer surfaces. Second, at the process development level, it is important to know the density of reactive neutrals and ions in complex chemistry, along with their flux on wafers. Morphology and surface characterization methods that could provide structural and chemical information at nanometer and subnanometer levels are also desired. These data, coupled with appropriate models, could reduce learning cycles and accelerate hardware and process innovations.[194] Last, at the production monitoring and control level, plasma and surface diagnostics that could provide wafer processing and tool stability information, such as etch endpoint,[217] arc detection,[218] wall degradation,[188] particle counts on wafer, and chamber fingerprinting[219] are of great importance. To avoid chamber contamination and interference with production, monitoring diagnostics need to be nonintrusive.

Second, purposely constructed experimental apparatus that could generate beams of neutrals, ions, electrons, and photons at specific energy, along with proper surface analysis methods can provide insights in plasma-surface interaction and the data needed for surface modeling. Early beam experiments[220] have provided seminal learnings on how reactive species interacted with surfaces, and the insights are still actively applied in current process designs. A modernized version of such an experiment that could dissect the unwieldy mixture of plasma into its components would help understand the individual and combined effect of reactive species on surfaces. One recent example of such work was performed by Lin *et al.*[180] who separated electron beam and studied electron-induced etching with CF_4/O_2 remote plasma. However, beam experiments often investigate surface interaction at the steady state, and its direct application in interpreting results from highly dynamic etch processes such as pulsing should be carefully examined. More discussion of the beam approach can be found in Sec. II J.

In addition, many recent breakthroughs in plasma etch can be somewhat attributed to the orthogonal control of neutral, ion, and electron beams. For example, plasma-based ALE separates reactive neutral delivery and energetic ion bombardment into a two-step cycle, which offers unprecedented etch selectivity and uniformity.[221] Introducing deposition processes in etch chambers[13] can also be understood as having separate control of neutral deposition. The direct current superimposed capacitively coupled plasma technology by TEL utilizes high-energy ballistic electrons for hardening EUV resist and mitigating patterning defects.[222] The various pulsing schemes, to a certain degree, also modulate the flux and energy of reactive species delivered on surfaces.[185] There are many unexploited beams of reactive species, such as photons,[223] gas cluster ion beam,[224] epitaxy beams,[225] that could offer significant performance boost in plasma etch.

3. Challenges in simulation, smart tool, and sustainability

Modeling and simulation have been proven effective in providing insights and mechanistic understanding of the complex behavior of plasma and surface processes. Their role in bridging the knowledge gap between in-feature etch metrics (ER, selectivity, etc.) and hardware/process input variables (power, flow rate, etc.) is tremendously valuable to equipment vendors.[209] To achieve this at a wider scale, and eventually accelerate process development, advancements in both plasma and surface modeling, of equal importance, are needed. Although the lofty goal of matching simulation conditions (of interpretive value) with experiments is often stated, we found that such situations rarely exist due to prohibitive computational cost and/or fundamental data availability. So far, most simulations are performed for special cases by experts using software built for particular applications. To increase industrial adoption, physical models, source code, and high-performance computing hardware need to evolve in pace with the ever-changing semiconductor industry. The continuous introduction of new materials and gas chemistries also demands corresponding data, such as cross section/rate in the gas phase and interatomic potentials at the surface, to become available in time.[194] As discussed in Secs. II O and II P, the combination of multiple simulation tools that bridges various length and time scales might provide the missing correlation from process knobs to on-wafer and potentially device results. However, the propagation of error through the long chain of models in such a system needs to be studied and properly addressed.

Mass production requires successful plasma etch tools and processes to run uniformly, stably, and repeatably on thousands of wafers with minimal performance drift and tool down times (Fig. 25). Particles and foreign elements introduced by processing equipment can cause random yield loss and should, therefore, be closely monitored and constrained.[188] Due to its highly corrosive nature, processing plasma constantly consumes chamber parts, such as wall, chuck, and focus ring, which will require replacement eventually. For these reasons, hardware design also involves the consideration of material compatibility, heat/temperature management, RF power generation and delivery, impedance matching,

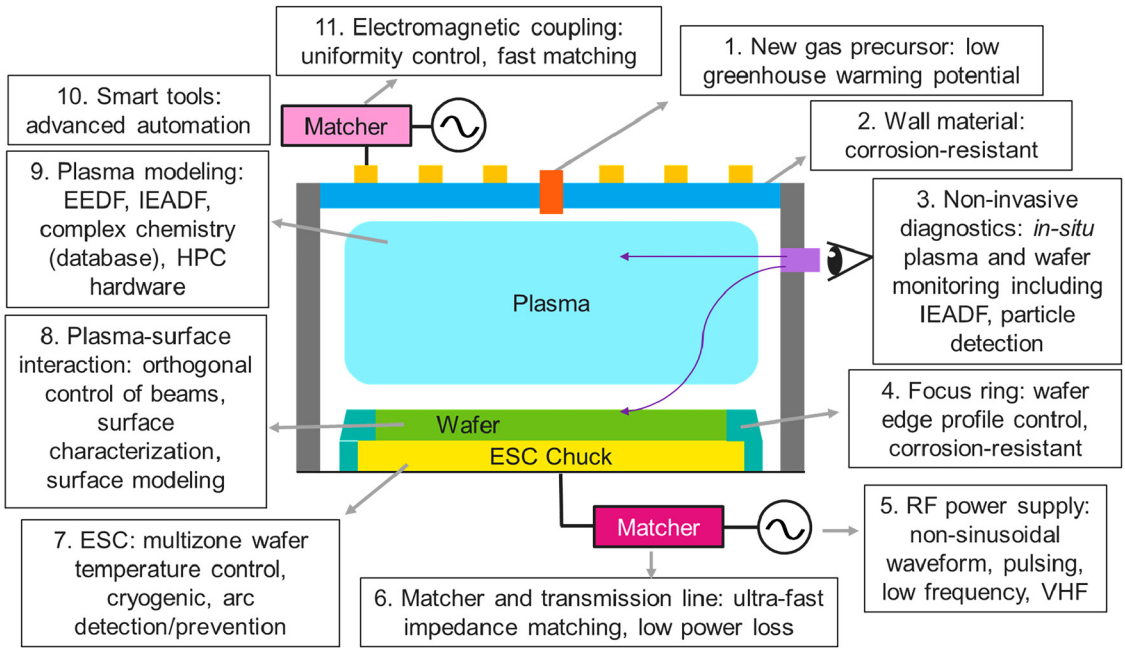

FIG. 25. Diagram of a plasma processing chamber showing where development is needed for mitigating future challenges of device scaling and new architectures. ESC, electrostatic chuck; EEDF, electron energy distribution function; IEADF, ion energy and angle distribution function; HPC, high-performance computing; VHF, very-high frequency.

electromagnetic interference control, manufacturing tolerance, maintainability, etc. Without giving an exhaustive list, we point out some current and future directions:

- real-time process control: advanced diagnostics that could monitor etch performance drift in real-time, and sophisticated algorithms that could adjust the associated tool parameters accordingly;
- smart tools that monitor part consumption, and automatically perform compensation and/or part replacement without vacuum break—machine learning of process log metadata can be a productive method;
- running cost reduction per wafer by increasing throughput, extending part lifetime, and reducing cleanroom footprint;
- tool upgrade cost reduction: modular hardware systems that are compatible within recent generations for easy upgrades;
- integration of advanced deposition methods including ALD, CVD, and epitaxial growth on etch tools; and
- sustainability: processes with reduced greenhouse gas emission and hardware with reduced helium and energy consumption—we must adopt a holistic view on efficiency and consider whole supply chain rather than one or two individual factors.

At the current stage of plasma etch development, many of the challenges mentioned in this section are shared among vendors, IDE/Foundries, and academia. Collaborative effort with effective leadership pinpointing the common issues, such as fundamental data, diagnostics, RF power generators, alternative etch gases, and efficient simulation frameworks, is expected to raise productivity and accelerate development for all.

J. Analyses of plasma-surface interactions for dry-etching processes

Satoshi Hamaguchi, Kazuhiro Karahashi

1. Overview

In plasma etching processes, surface atoms are removed by knock-on collisions with incident energetic ions and/or by the formation of volatile species through chemical reactions at the surface with the chemical species generated in the plasma. As many physical and chemical processes occur simultaneously in plasma-surface interactions, it is often difficult to identify the most essential etching mechanisms. In this section, we discuss how plasma-surface interactions can be analyzed for a better understanding of the fundamental mechanisms of dry-etching processes.

Coburn and Winters demonstrated in the late 1970s that the fundamental mechanism of silicon (Si) etching with fluorine (F)-containing plasmas can be understood as a synergistic effect of the chemical etching reactions of Si by F atoms and physical sputtering by incident energetic Ar ions, using beam experiments, rather than plasma experiments.[142] Because the nature of the incident ion beam can be characterized with high accuracy, beam experiments are key to a good understanding of the elementary processes of plasmas-surface interaction in general.[226]

Figure 26 shows an example of a mass-selected ion-beam system used to evaluate the etching yields (or sputtering yields, i.e., the

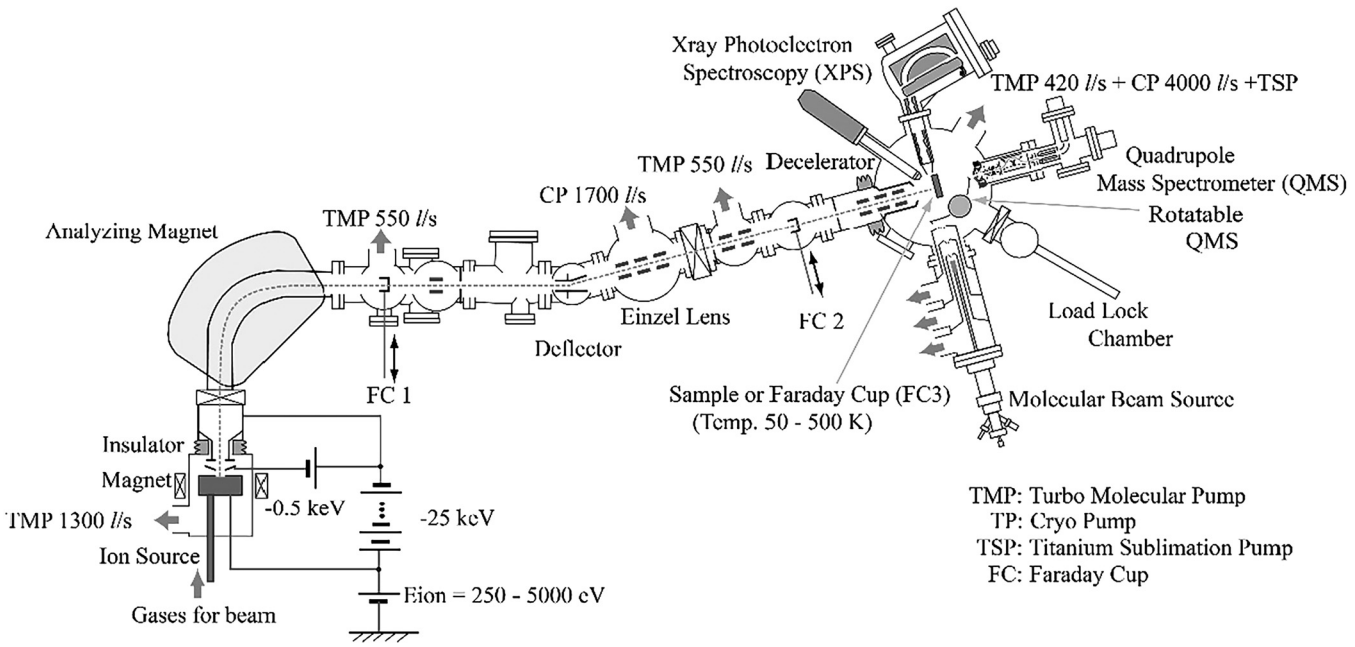

FIG. 26. Schematic diagram of a mass-selected ion-beam system to study beam-surface interactions under high-vacuum conditions. For more details, please refer to Ref. 227.

number of specific atoms removed from the surface per ion injection) of various materials for semiconductor process applications.

As Coburn and Winters demonstrated, etching effects are typically not additive or cannot be expressed as a superposition of known elementary etching processes. Therefore, even if we understood the synergetic effects of all possible combinations of two or three elementary etching processes, we might never fully understand realistic etching processes, where a large number of elementary etching processes (e.g., ion impacts and surface chemical reactions with various gaseous chemical species) occur simultaneously. Nevertheless, in practice, a better understanding of some essential elementary surface reactions and their synergetic effects helps identify the most dominant etching mechanisms.

The energy dependence of the etching yield is often of great interest in developing new dry-etching processes. For the etching yields of single-element materials by single-element ion impact, a large amount of data has been accumulated[227] for a wide range of ion kinetic energies. For semiconductor process applications, the etching yields of binary component materials such as SiO_2 and SiN by chemically reactive multicomponent ions such as CF_3^+ are also of interest, but such etching yield data are still limited.[228–231]

Theoretical study of plasma-surface interactions can be performed with MD simulations[176,232,233] and DFT simulations.[234,235] Figure 27 shows an example of the etching yield evaluation of Si and SiO_2 by SF_5^+, $C_2F_5^+$, NF_2^+, and F^+ ions as functions of the ion incident energy, obtained from MD simulations. With the advancement of computational resources and parallel computing technologies, large-scale simulations have become more manageable recently. As the size of semiconductor devices shrinks, the entire device structure may be simulated as a collection of atoms in the near future.[236,237]

AI and ML,[60,238] see Sec. II M, also play important roles in predicting some aspects of plasma-surface interactions (see Sec. II P). For example, based on large databases of etching yields, the etching yields of materials can be predicted with ML.[239–241] ML can be also used to model the interatomic force fields of classical MD simulations based on a large amount of atomic-interaction data obtained from DFT calculations.[242] The use of AI and ML is expected to contribute significantly to the analysis of plasma-surface interactions, combined with conventional scientific analyses.

2. Challenges and roadblocks

The major challenges and roadblocks to the development of new plasma processes are the lack or shortage of fundamental data on elementary interactions between the gaseous species and surfaces, including etching yields, and the gas-phase collision cross section and reaction rate data. For example, fundamental surface and gas-phase reaction data constitute the most basic building blocks of full-scale numerical simulations of plasma etching processes such as the evaluation of the profiles of etched or deposited surfaces.[243,244] For such simulations, one would need the energy and angle dependence of the etching yields of the surface materials for every incident ion species and other data on the interactions of incident species and surfaces, in addition to gas-phase collision and reaction rate data for plasma simulations. Since every surface can be considered special (as a function of feature location and time),

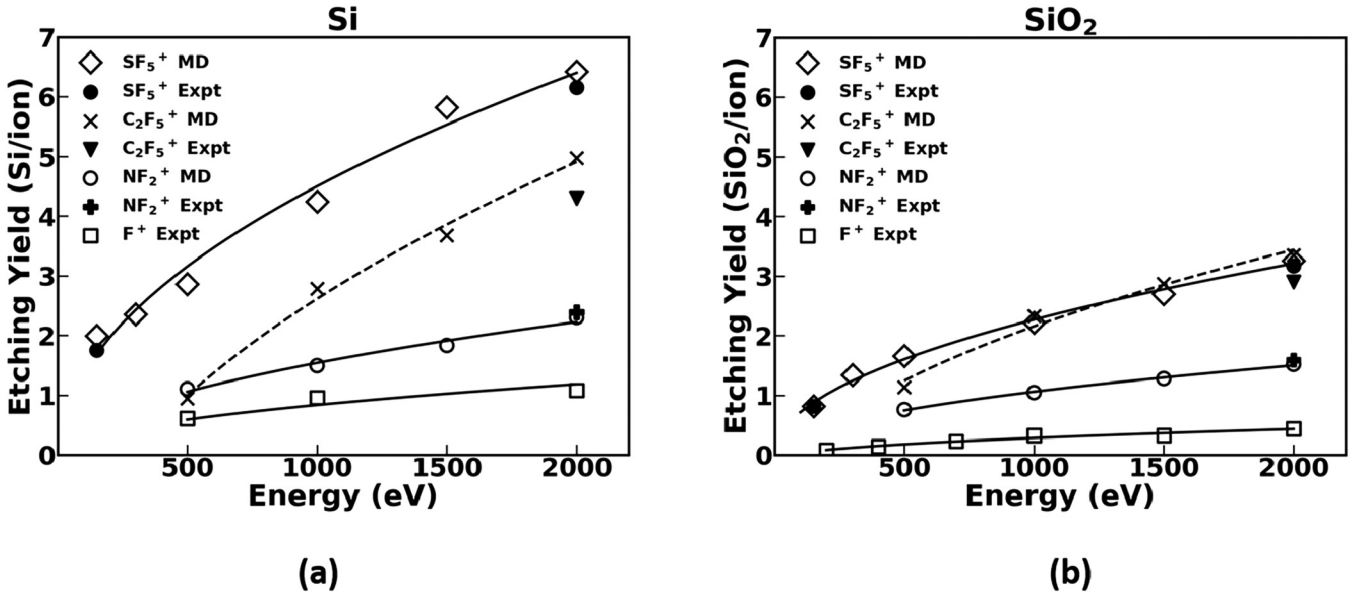

FIG. 27. Etching yields of Si (a) and SiO2 (b) by SF5+, C2F5+, NF_2+, and F+ ions as functions of energy obtained from MD simulations (denoted as "MD") and compared with the experimental data ("Expt"). This figure was modified from that in Ref. 233 [Reprinted with permission from Tinacba *et al.*, J. Vac. Sci. Technol. B **39**, 043203 (2021) (Ref. 233). Copyright 2021, American Vacuum Society]. The simulation and experimental data for C2F5+ and NF_2+ are from Ref. 233, the experimental data for Si by F^+ ions are from Ref. 229, and SiO_2 by F^+ ions from Ref. 230.

we need etch yields as a function of specific surface compositions to be able to fully predict feature evolution. For instance, we need etch yields as a function of degree of halogenation or other pertinent parameters.

3. How to overcome the challenges and roadblocks

However, it is practically impossible to collect such fundamental data for all possible combinations of materials and incident gaseous species in advance. Therefore, a desirable and practical solution to assist new process development would be to have a high-throughput screening (HTS) system for the experimental measurements of plasma-surface interactions ready to operate and to perform fundamental experiments relevant to the process development promptly when there is a need for such data. The HTS system should be equipped with a beam system similar to the one shown in Fig. 26, but the beam irradiation and surface measurements need to be made automatically with little human intervention for efficient operations. Similarly, close collaborations among producers of fundamental gas-phase data and users of such data are needed to obtain promptly the fundamental collision cross section and reaction rate data for new gas chemistry.[245]

To ensure the reliability of the obtained data, we must verify the consistency between the experimental data and theoretical predictions whenever possible. There have been some attempts to predict the values of missing data using AI and ML techniques,[238] but how these efforts will contribute to the development of new processes is yet to be seen.

4. Outlook

As discussed above, the development of specialized experimental systems, such as the HTS system discussed above, to determine fundamental surface and gas-phase reaction data experimentally is one of the most important future research directions for more efficient development of new plasma processes. The number of "process knobs" (i.e., process conditions that can be used for optimization of semiconductor device manufacturing) is said to be increasing exponentially. Therefore, unlike in the past, a near-exhaustive search for optimized process conditions is currently impossible. Reliable and well-curated data of surface and gas-phase interactions in plasmas help the process developer explore the most promising directions swiftly.

To provide theoretical support for a better understanding of plasma-surface interactions, multiscale simulations, i.e., simulations covering multiple spatial and temporal scales from atomic motion to plasma dynamics, are of significant importance for practical applications (see Sec. II P). For example, the theoretical/computational prediction of etched profiles under given plasma conditions requires micro/nanoscale profile simulations coupled with macroscopic sheath and plasma simulations. For MD simulations to reveal atomic-scale plasma-surface interactions, the interatomic forces must be accurately modeled based on quantum chemical simulations. Typical DFT simulations cannot model the excited states of atoms and molecules, but quantum-mechanical simulations including excited states—e.g., Time-dependent density-functional theory (TDDFT)—are likely to be needed to better account for plasma-surface interactions with electronically excited species (such as metastable species) when the energy transfer from electronically excited species to the surface cannot be neglected. TDDFT can handle excited states but is far from applicable in the mainstream, and low-energy electron interactions require development.

Finally, AI and ML are expected to play important roles in optimizing the design of experiments as well as predicting missing surface and gas-phase reaction data based on the available experimental data as well as numerical simulations. The establishment of "virtual metrology" of plasma-based semiconductor processing tools, such as dry etchers, is one of the ultimate goals of research in this field, to achieve real-time process control and process development for next-generation manufacturing. Here, "virtual metrology" refers to the prediction of the surface and gas-phase conditions of semiconductor manufacturing tools based on data obtained from the numerical simulation of the computational models of the tools (i.e., digital twins), as well as available real-time data collected from the processing tools during operation. The development of virtual metrology systems requires various AI and ML techniques coupled with a deep understanding of the underlying physics of plasma processes.[238]

K. Plasma VUV effects, doping effects, and related topics

Vincent M. Donnelly

1. Overview

In anisotropic plasma etching for pattern transfer into microelectronics materials, it is well established that energetic positive ions accelerated through the plasma sheath and impacting the surface at near normal incidence, initiate chemical reactions, and desorption of products and/or inhibiting films, leading to vertically directed etching of exposed areas through a photolithographically defined mask.[2,142] As critical components of integrated circuits proceed to ever thinner layers, *low-energy* ion stimulated etching will be increasingly called for. The etching yields (substrate atoms/molecules per incident ion) decrease at low energy. This potentially leads to new phenomena that could compete with ion-driven anisotropic etching. Among these, photons have been shown to promote etching of silicon in halogen-containing plasmas under some conditions. Higher energy photons can also cause damage that is often sensed by degradation of a device electrical characteristic.[246–249]

2. Challenges

There seem to be two distinct classes of photoassisted etching. The first is characterized by low yields of typically 10^{-4} substrate atoms per photon. Many studies of silicon etching have been carried out in halogen gas atmospheres with lamps or lasers in the *absence of a plasma*. For example, Okano *et al.*[250] found that semi-insulating and *p*-type Si could be etched with Cl atoms produced by photodissociation *plus* surface irradiation with UV or visible light. Etching was ascribed to creation of electron-hole pairs that promoted surface reactions. Etching of masked samples produced relatively smooth surfaces, with little mask undercutting, though etched sidewalls are often sloped. Kullmer and Bäuerle carried out similar studies with Cl atoms generated by photodissociation of Cl_2

with a 308 nm XeCl laser parallel to the surface and surface irradiation with a Kr^+ laser at 647.1 nm.[251] They also attributed etching to photogenerated carriers. Sesselmann *et al.* carried out similar experiments with excimer lasers at 308 and 248 nm, ascribed the wavelength dependence at low laser fluence to photodissociation of Cl_2 gas and the efficient photodesorption of silicon chlorides.[252] Houle investigated Si etching by XeF_2 with 515 nm Ar^+ laser and concluded that photostimulated desorption of SiF_3 is the rate controlling etching step, stimulated by a chemical reaction involving photoinitiated charge carriers.[253]

Ion-assisted etching yields (substrate atoms per ion) are typically ~0.1 just above threshold for inducing etching, to ~5–10 at ion energies near 500 eV. While plasmas generate visible and UV light, these photons impinge on the substrate with fluxes at least an order of magnitude lower than positive ions. Consequently, UV/visible photon-induced etching does not compete with positive ion-assisted etching, even with ion translational energies of only a few eV above the threshold.

A second, less reported class of photoassisted etching is characterized by yields well in excess of unity. Such high photoassisted etching yields are only obtained with much higher energy photons in the vacuum UV (VUV) wavelength region below ~150 nm. Schwentner and co-workers have investigated photoassisted etching Si in the presence of $XeF_{2(g)}$, as well as GaAs with $Cl_{2(g)}$, using VUV light produced by a synchrotron.[254,255] In both cases, the etching yields increased dramatically with decreasing wavelength and reached an improbable ~100 substrate atoms etched per photon between 130 and 110 nm. Since most photons penetrated more deeply, the efficiency per absorbed photon at the surface was of the order of 10^5. These incredibly high yields were attributed to unspecified chain reactions. Yields above unity were also reported for Cu etching in the presence of Cl_2 gas.[256]

With such high yields, VUV photons generated in the plasma can, therefore, compete with ion-assisted etching, especially with low ion energies. Surfaces exposed to a plasma will absorb most of the light escaping the plasma. VUV photon fluxes ranging from 1×10^{15} to 1×10^{17} photons/cm^2 s have been reported at the edges of Ar ICPs.[257–263] These fluxes are comparable to those for positive ion bombardment of the substrate. Fast photoassisted etching of p-type Si(100) and poly-Si has been found in Ar inductively coupled plasmas containing Cl_2, HBr, and mixtures of Cl_2 and HBr.[181,264–267] In these studies, etching rates decreased with decreasing ion energy until reaching the threshold for ion-assisted etching, whereupon, the etching rate became independent of ion energy.

Photon-assisted etching of Si is often explained with the aid of energy band diagrams, such as those in Fig. 28. E_V and E_C are the energies at the valence and conduction band edges, E_i is the intrinsic energy level, E_F is the Fermi energy level, and V_p is the plasma potential. The work function, electron affinity level, and vacuum energy level are indicated by the symbols ϕ, ψ, and E_{VAC}, respectively. A^- and D^+ represent immobile acceptor and donor ions. The conduction and valence bands bend up or down at the surface if defects pin the surface Fermi level near the midgap. In the absence of a plasma (i.e., no imposed electric fields or photons), negative ions (F^- and Cl^-) on the surface and near-surface region have been invoked to explain Si etching in fluorine and chlorine-containing plasmas, including the dependence of the etching rate on dopant number density and type.[268–270] Etching is believed to be enhanced by F^- and Cl^- being driven into the subsurface region by the electric field produced by the presence of negative ions, invoking a mechanism analogous to that proposed by Cabrera and Mott[271] to explain oxidation of Si. The presence of a plasma also can affect surface band bending, due to the electric field imposed by the plasma sheath, as well as positive ion and electron impingement. For a typical sheath width of 100 μm and sheath potential of 100 V (due to a typical DC self-bias resulting from an imposed radio-frequency stage bias), and assuming the entire voltage drop is between the plasma potential and the grounded sample, the electric field at the Si surface is ~10 kV/cm.

When a photon with energy in excess of the bandgap of the semiconductor (1.12 eV for Si) is absorbed, a free electron is created in the conduction band and a hole is formed in the valence band at a distance of typically 10–1000 nm below the surface, depending on photon energy and whether the excitation is across a direct or indirect bandgap. Minority carriers created in or diffusing to the near-surface depletion region can then move to the surface, due to band bending, and cause etching, as well as some band flattening. When a 104 nm (11.92 eV) photon produced in an Ar plasma is absorbed by Si, the electron-hole (e-h) pair created possesses 11.92–1.12 = 10.8 eV of excess energy. The initial, hot carriers lose this energy and produce about three additional e-h pairs.[272–274] Hot majority carriers can overcome the repelling electric field and reach the surface. None of these effects can produce yields in excess of unity, let alone 100. Therefore, etching yields for carrier-driven etching by VUV photons can seemingly be ruled out as the main mechanism.

Consequently, a high-energy photochemical process more likely initiates etching. Since the yields greatly exceed unity, the process must be catalytic and more complicated than a simple photon-stimulated desorption process. One proposed mechanism is a photocatalytic chain reaction, initiated by desorption of a negative ion, which can only occur with high-energy photons. The remaining positive charge (i.e., hole) leads to the weakening of an Si–Si bond at the surface and lowers the barrier for formation and desorption of SiCl and/or $SiCl_2$ etching product. The positive charge is left behind, where it can migrate to nearby Si–Si bonds and repeat the process many times before being neutralized by an electron or Cl^-. It should also be noted that such a mechanism can also occur for etching of metals and dielectric materials and perhaps is also occurring in the $CuCl_x$ layer during copper etching with synchrotron radiation.[256]

The complex interactions between plasmas and semiconductor surfaces are not well understood. All of these effects are further influenced by the thickness and composition of the etching surface layer containing electronegative species and perhaps negative ions. Furthermore, the degree of band bending depends on dopant concentration and light intensity and can also be altered by large sheath potentials. The ion bombardment that causes etching also modifies the surface and influences the photoeffects. Therefore, careful experiments to isolate the effects of dopant types and concentrations, photons, ions, electrons, and adsorbates, combined with advanced theory will provide needed insights into this poorly understood aspect of plasma processing of semiconductors.

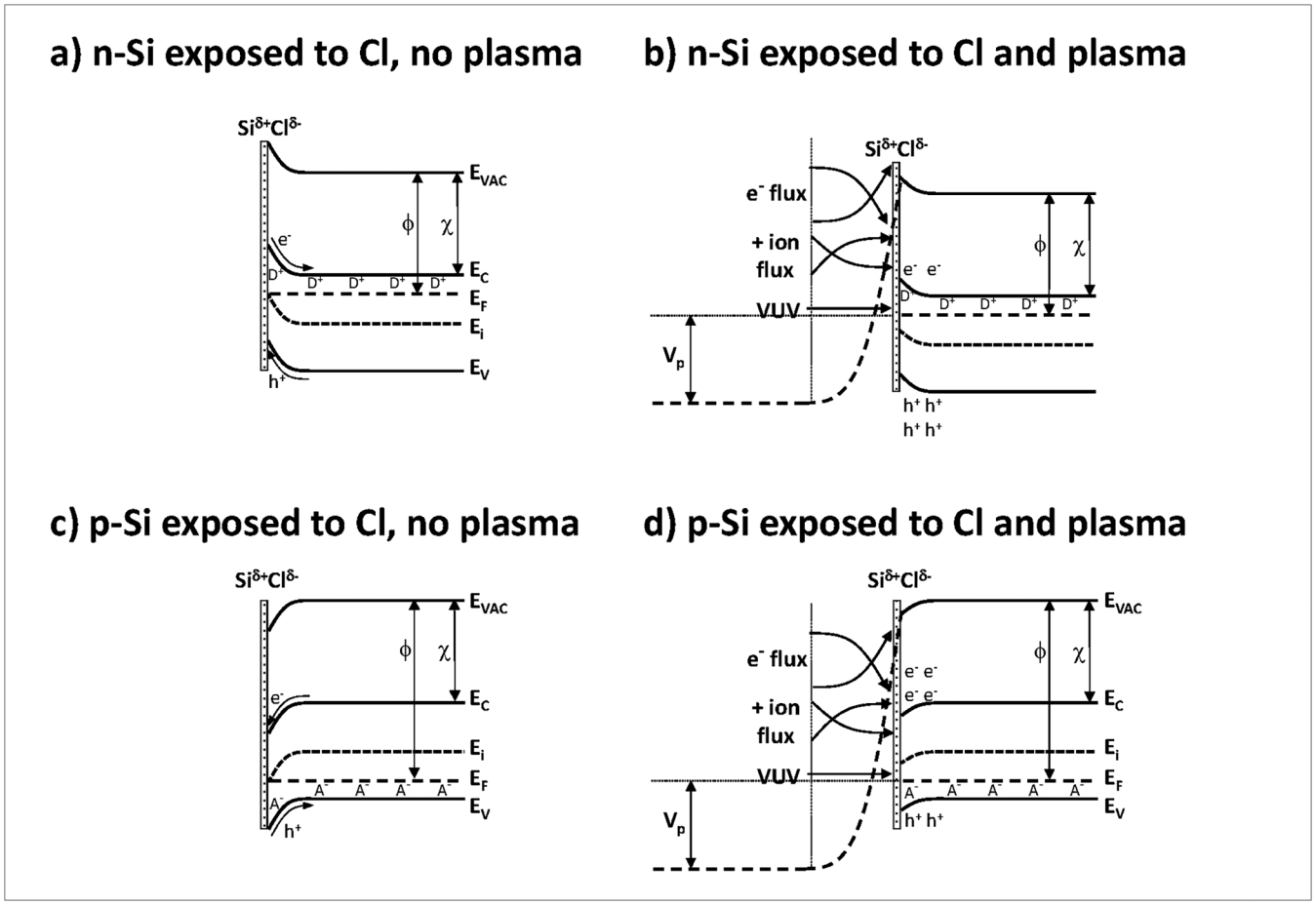

FIG. 28. Qualitative band diagram near the surface of chlorine-exposed *n*-type and *p*-type Si in the absence of a plasma (a) and (c), respectively) and for *p*-type Si in the presence of a plasma (b) and (d), respectively). Reprinted with permission from Linfeng Du, Demetre J Economou, and Vincent M Donnelly, Journal of Vacuum Science & Technology B 40 (2), 022207 (2022). Copyright (2022) American Vacuum Society (Ref. 181).

3. Outlook

Plasma VUV-induced etching is not just of academic interest but is also vitally important for future plasma processing. It has been found that etched profiles can have a variety of shapes from vertical narrow trenches near mask edges [Fig. 29(a)] to nanoholes transferred from a native oxide masked hole pattern [Fig. 29(b)], to crystallographic [Fig. 29(c)], where (111) planes etch much slower than (100) planes. The causes for such varying profiles are not well understood. Etching of ~10 nm diameter or smaller holes with 100 nm photons suggests that surface plasmons might play a role in light propagation down the sides of conducting features, a topic that could benefit from theory development. The ability to etch even deeper nanoholes without energetic ion bombardment could have important applications.

It is perhaps more likely that conditions promoting photoassisted etching, resulting in nonideal etched profiles such as those in Figs. 29(a) and 29(c), will need to be avoided. Also, in atomic layer etching, it is desirable to carry out the etchant chemisorption steps in the presence of a plasma to maximize coverage and, therefore, etching yield in the subsequent ion bombardment steps. No etching (ion or photon-assisted) should occur during the chemisorption step. Consequently, a more thorough understanding of VUV production, transport in the plasma, and methods for reducing VUV production are needed.

L. Atomic layer etching and ultrahigh materials etching selectivity

Andreas Fischer, Thorsten Lill

1. Status and promising developments

ALE builds upon the principles of ALD, a technique that is widely used in semiconductor fabrication. ALD involves a

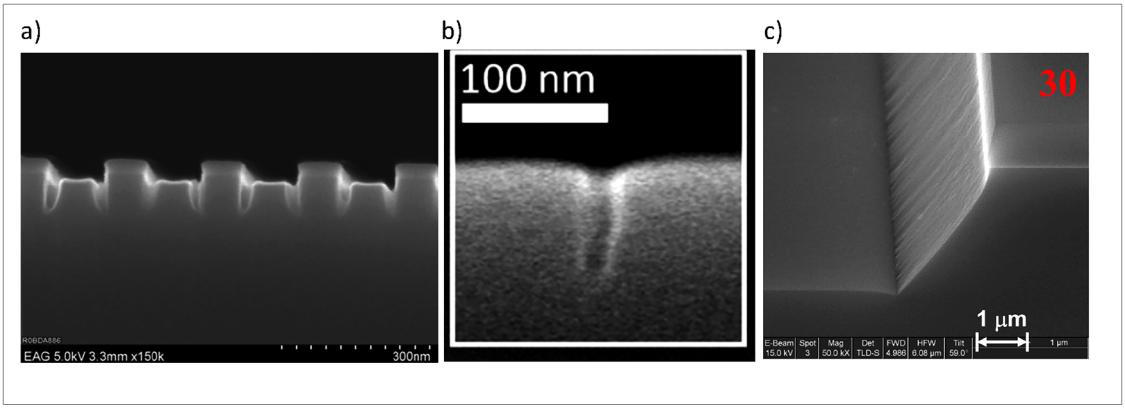

FIG. 29. (a) VUV assisted etching of silicon (100) in a 1%Cl_2/Ar pulsed, Faraday-shielded ICP (ion energy <10 eV) at 50 mTorr. Reprinted with permission from Shin *et al.*, J. Vac. Sci. Technol. A **30** (2012). Copyright 2021, American Vacuum Society (Ref. 266). (b) VUV assisted etching in the downstream region of a Cl_2 microwave surface-wave plasma with no substrate bias and an ion energy of ~3 eV. Nanoholes were etched through a native-oxide masked hole pattern. Reprinted with permission from Tian *et al.*, J. Vac. Sci. Technol. B **33** (2015). Copyright 2015, American Vacuum Society (Ref. 277). (c) Etching in a Faraday-shielded 4% Cl_2/Ar ICP (ion energy <10 eV) aided by VUV light in the plasma an additional VUV light from an Ar/He ICP. Reprinted with permission from Du *et al.*, J. Vac. Sci. Technol. B **40**, 022207 (2022). Copyright 2022, American Vacuum Society (Ref. 181).

sequential exposure of a substrate to alternating precursors, resulting in the controlled growth of atomic layers.[276] ALE, on the other hand, aims to selectively remove atomic layers with atomic-scale precision. Similarities and differences between both ALD and ALE were illuminated by Faraz *et al.*[277] Yoder's U.S. patent 4756794 published in 1988 is considered the earliest report on this etching technology.[278] Figure 30 shows a schematic of the generic ALE concept. Modification and removal steps are self-limited. Surface modification methods include adsorption, diffusion, implantation, conversion, deposition of a reactive layer, extraction, and potentially other methods. The successive removal of the modified surface layer can be activated with either accelerated ions and neutrals, electrons, photons, thermal energy, or chemical reactions. These methods may be combined and may be performed thermally or plasma-based leading to a potentially large number of different ALE techniques.

Plasma-enhanced ALE has been studied for over 30 years.[31,172] About a decade ago, it became evident that commercial plasma etch reactors could be adapted to perform plasma-enhanced ALE.[280,281] This triggered a resurgence of research on this class of ALE. Separation of the etching process into self-limited surface modification and removal steps enables enhanced etching uniformity across the entire wafer and a decrease in ARDE.[31] ALE processes produce, in most cases, a smooth etch front.[143,282] From a scholarly perspective, plasma-assisted ALE enhances our comprehension of RIE, its continuous etching analog.

In 2015, researchers at Intel formulated the so-called "four-color challenge" in advanced semiconductor manufacturing. It

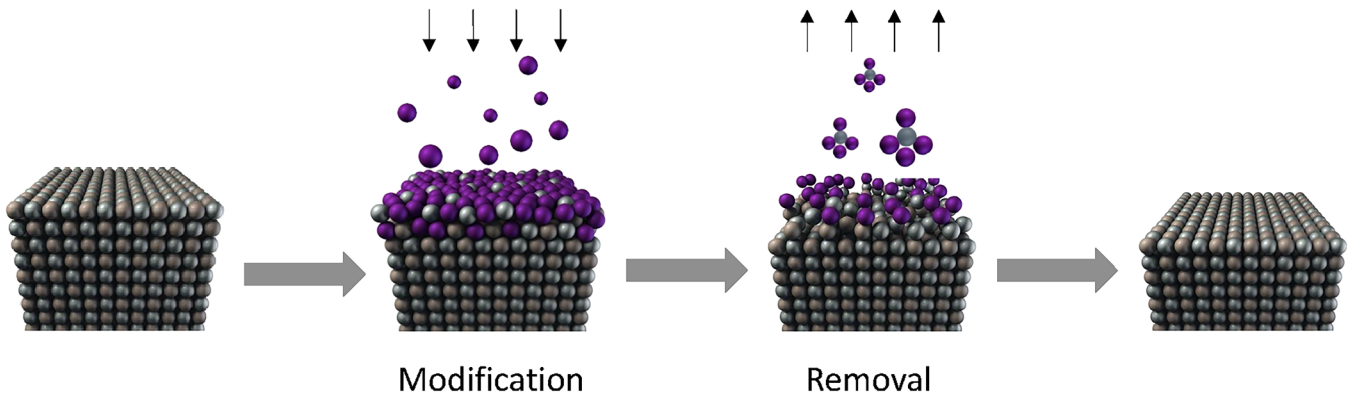

FIG. 30. Schematic of the generic ALE concept.

reflected the need for near infinite etch selectivity among a wide range of materials.[283] In the same paper, the authors introduced the concept of an extremely selective ALE processes, which uses only chemical reactions at thermal energies. First experimental results on thermal ALE were published in in the same year.[284–287] Since then, publications about thermal ALE processes have steadily increased in frequency from less than a total of five before 2015 to typically more than 25 per year now.[288] Thermal ALE processes have been found for many materials in rapid succession and were summarized in recent reviews.[289,290]

Plasma-enhanced ALE in which either the modification or the removal step uses ions from an *in situ* plasma is also called directional ALE. The directionality is brought upon the process by the orientation of a plasma sheath, which accelerates ions perpendicular to any plasma-wetted surface. Directional ALE is an established etching technology in the semiconductor industry. It uses oxidizing gases such as halogens or oxygen with and without plasma activation to form a weakly bonded surface layer. Ideally, ions with a carefully controlled kinetic energy sputter just this weakened layer but not the unmodified material below. This careful control is the origin of etch selectivity in directional ALE.[291] In some industrial etch applications, a combination of classic RIE and ALE is used. For example, RIE can cover the "main etch" step of the process, whereas ALE methods are employed in a "soft-landing" step or to perform a selective "over etch" step with low damage.

The application space of directional ALE is, however, still small compared to classic RIE. Among the reasons are low throughput and the attenuation of low energy ions inside high-aspect-ratio structures. High ion energy directional ALE expands the list of potential ALE applications.[292,293] In this method, an ion energy above the sputter threshold of the bulk material is used, but the step time is reduced to limit the loss of the unmodified layer. Uniformity and ARDE benefits can still be achieved in such a process but selectivity loss and plasma damage must be carefully controlled. High ion energy ALE bears resemblance with mixed mode pulsing where the plasma power and gas flows are cycled.[294]

Among the first semiconductor manufacturing applications of directional ALE was self-aligned contact etching of silicon oxide with alternating fluorocarbon and argon plasma.[221,295,296] Employing ALE enables high silicon oxide to silicon nitride selectivity while maintaining excellent contact open performance. Another application is the etching of 3D fin field-effect transistor (FinFET) gates[297] where a typical RIE process often leaves Si residues at the base of the fins. Silicon ALE with chlorine plasma in the modification step and argon plasma for removal shows promise to solve this challenge. Directional ALE has also been demonstrated for etching of metallization lines for logic devices. In one report, the copper was oxidized with a biased plasma and the copper oxide was removed with formic acid vapor.[298]

The observation that ALE can smoothen surfaces during etching while being very selective sparked research work to use it for patterning with EUV resist. Superior line-edge roughness performance was observed when the antireflective layer underneath the EUV resist was opened with directional ALE instead of RIE.[299] Changes in the final critical dimension were more uniform across all features when ALD deposition steps were added.[299] Furthermore, directional ALE has been demonstrated for double patterning or pitch splitting,[300] respectively.

Advanced RF and power devices require low damage etching of GaN, AlGaN, and similar materials. Directional ALE[301–303] and plasma-enhanced isotropic ALE (Ref. 306) are considered for these applications due to their excellent damage performance and high selectivity.

Although the majority of etch applications have traditionally been directional, isotropic etching is increasingly required. Thermal isotropic ALE can be understood as a cyclic implementation of radical or vapor etching processes.[305] In semiconductor device manufacturing, thermal ALE arises as a critical technology for 3D memory and logic devices such as advanced 3D-NAND, emerging 3D DRAM, and vertical logic transistor structures.[306] The manufacturing of these devices involves highly selective etching in vertical and horizontal directions inside structures with extremely large aspect ratios.

Several key advantages compared to RIE or directional ALE exist that will promote its deployment:

1. The etch front propagates in all directions such that lateral etching can be achieved. Places underneath overhanging features can be etched.
2. Materials that have byproducts with high melting points can be etched.[307–310] These materials are difficult to remove with RIE.
3. Mechanical, photonic, and electrical etch damage of the devices is eliminated as both ALE steps are based on thermal reactions. Chemical damage especially for higher surface temperatures must be controlled.

Compared to continuous mode selective isotropic etch technologies such as radical and vapor etch, thermal ALE has the following advantages:

1. When operated in full saturation mode, transport-related phenomena such as center-to-edge etch nonuniformities across the substrate or inside structures as well as feature size loading can be mitigated.
2. The etch chemistry can be greatly simplified due to the self-limiting character of the processes.

A number of advanced etch applications are being explored in which ALE processes would show benefits. One such potential application is etch-back of tungsten and TiN.[311–313] from the sidewalls or shelve overhangs in 3D-NAND structures. An example of a 3D memory test structure in which HfO_2 is recessed is displayed in Fig. 31. It was determined previously that owing to the relatively low sticking and reaction rates of HF on an HfO_2 surface, uniform lateral etch rates top-to-bottom can be achieved in these holes for most HF doses.[279]

Combinations of ALD and ALE have been shown to enable thin, smooth layers with a crystalline structure by first achieving crystallinity in depositing a thicker, defect-free film and then reducing its thickness via ALE while retaining its crystalline structure.[314] This capability is important for the formation of capacitor dielectrics in DRAM devices.

A critical logic device etch application example was demonstrated by Lu *et al.*[315,316] They built a successful GAA structure with InGaAs nanowires using thermal isotropic ALE. This resulted in an FET device that was fully functional. The transmission electron microscopy (TEM) of the final structure is shown in Fig. 32.[315]

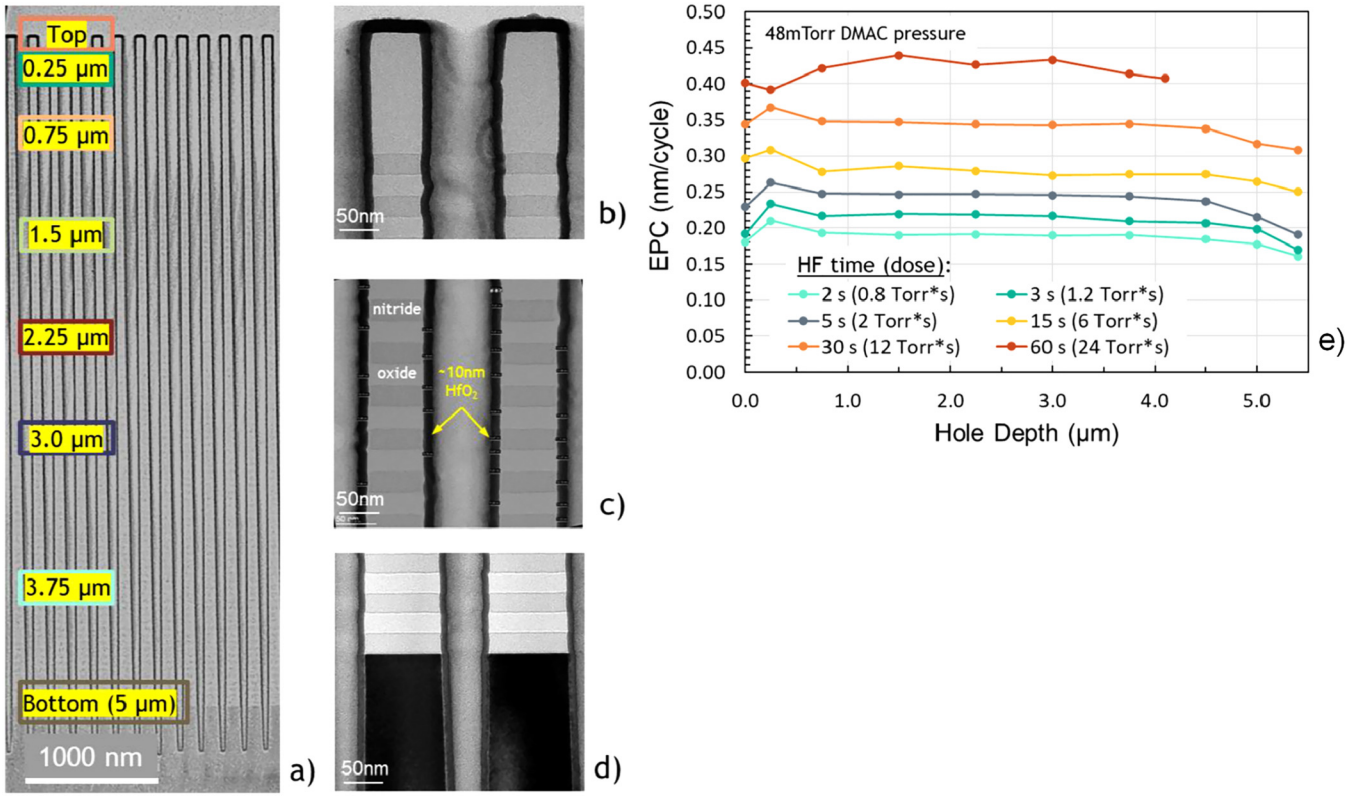

FIG. 31. Cross section and close-ups of a full 5 μm deep ONON stack prior ALE [(a)–(d)]. EPC profiles for HfO_2 films in the same structure using various HF dosing (time) and a constant Dimethyl aluminum-chloride (DMAC) exposure at 350 °C. The lateral EPCs remained uniform top-to-bottom inside a hole for each HF dosing condition (e). Reprinted with permission from Fischer *et al.*, J. Vac. Sci. Technol. A **40**, 022603 (2022). Copyright 2022, American Vacuum Society (Ref. 281).

Furthermore, the ability to etch nonvolatile materials makes thermal ALE a candidate for patterning of magnetic random access memory and spintronic devices.[307,308,317]

2. Unresolved issues and challenges

Directional and thermal ALE are emerging etching technologies that meet the needs of advanced semiconductor manufacturing with atomic level fidelity by enabling the shaping of 3D structures. Directional ALE leverages the tools and experience from many decades of RIE, the workhorse of the industry. Thermal ALE is a powerful selective isotropic etch tool that augments radical and vapor etch solutions. It enables a wider range of materials to be etched and addresses ARDE challenges of its continuous process counterparts. To fully realize the promise of both types of ALE, several challenges must be solved:

1. In directional ALE, a narrow gap chamber would be beneficial as it reduces the gas residence time above the wafer allowing faster switching between steps and, ultimately, higher

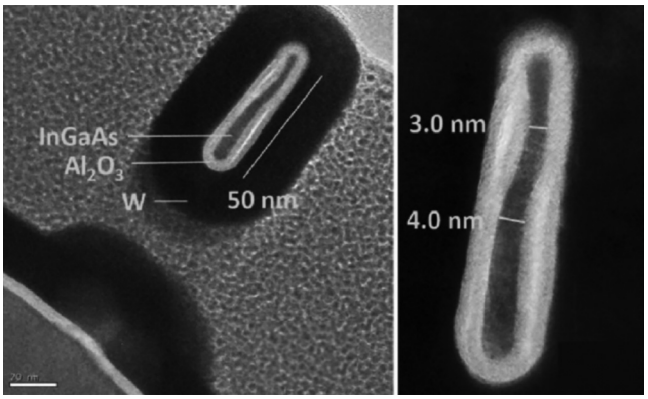

FIG. 32. TEM cross sections of a 4 × 50 nm InGaAs nanowire covered by 4.7 nm ALD-grown Al_2O_3 and 20 nm of ALD tungsten. Reprinted with permission from Lee *et al.*, in *International Electron Devices Meeting,* 1–5 December 2018 (IEDM, San Francisco), p. 895. Copyright 2018, IEEE (Ref. 318).

throughput. Low-gap chambers, however, are a challenge for inductively coupled plasmas as the proximity of the inductor to the substrate may result in electrical device damage.
2. Low-energy ions required in directional ALE applications may fail to travel deep into high-aspect-ratio structures due to scattering or recombination. High ion energy ALE may be a solution.[292,293]
3. Even if ALE removal rates of one monolayer per cycle were assumed, wafer throughput is significantly less than with RIE processes. Etch rates per cycle and thereby wafer throughput can be boosted by high dosing during each of the process steps, by increasing the substrate temperature if the device tolerates it, and by the use of plasma to increase the reactivity.
4. The need to boost wafer throughput brings about a trade-off with the inherently self-limiting nature of ALE reactions, as there may not be ample time for a surface to achieve chemical saturation. Consequently, nonsaturation can lead to undesirable effects such as nonuniform etching from the center to the edge of the wafer, issues with device uniformity from top to bottom, and loading effects related to feature size.
5. In the absence of plasma in both ALE steps, the process must be run at elevated temperatures, in some cases well above 200 °C. The high thermal strain may be an issue for some devices as it accelerates diffusion of atoms across material interfaces. Additionally, high temperatures may introduce parasitic chemical reaction paths, producing unwanted etch outcomes.
6. Another challenge relates to reaching an etching selectivity of over 100:1 between materials when they are chemically similar to each other. One such example was illustrated by Abdulagatov *et al.* when the etch selectivity between $Si_{0.15}Ge_{0.85}$ and Si was only 10:1.[318]
7. ALE precursors, especially those used in thermal ALE, are very reactive—they may react with residuals from the other ALE step, forming undesirable secondary reaction cross products and form wall deposits or powdery residues from reacting with leaked air. *In situ* plasma cleans or regular wet cleaning with an opened chamber may be one solution to this challenge. ALE at cryogenic temperatures has been demonstrated to have no chamber wall effects.[319]
8. The cost of some of the precursors used in ALE today is prohibitive for mass production.

Atomic layer etching has made significant strides since its inception in the late 1980s and has evolved into a diverse set of tools of etching techniques. Innovative processes continue to emerge, enabling the etching of novel materials and structures at a rapid pace. Both thermal and plasma-based directional atomic layer etching are on the verge of gaining widespread acceptance as essential extensions to the existing suite of etching technologies in semiconductor manufacturing. These methods are indispensable for contemporary and future device designs at the nanometer scale.

M. Plasma cryogenic etching

Rémi Dussart, Masanobu Honda

1. Introduction

Cryogenic etching was first introduced in 1988 by a Japanese team.[320] Today, this process is attracting renewed interest as the industry faces new challenges in the fields of memory and logic. Substrate cooling at low temperatures (well below 0 °C) offers new prospects for improving pattern dimensional accuracy, selectivity, and etch rate. Numerous improvements have been made, and it is now possible to reach quite low temperatures without liquid nitrogen, by using chillers, making cryogenic processes more attractive for industrial applications. Recently, a cryogenic process was used to deeply etch silicon oxide and nitride layers for 3D-NAND flash memories.[11]

2. Overview

Cryogenic etching can be used in different ways and for different applications. A schematic is provided in Fig. 33, illustrating some examples of utilization of cryoetching.

Cryogenic etching was first proposed to etch silicon vertically by freezing chemical reactions at the sidewalls.[320] Meanwhile, it was shown that high-aspect-ratio etching could only be achieved in the presence of oxygen mixed with SF_6 to form an SiO_xF_y passivation layer on trench sidewalls.[321] This first utilization is schematically represented in Fig. 33(a), showing the cross section of a deep silicon trench protected by an SiO_xF_y passivation layer, the composition of which is illustrated above the figure with the layer atomic composition. This SiO_xF_y passivation layer, which forms at low temperatures, mainly desorbs when the wafer is brought back to room temperature.[322] Its formation was studied using *in situ* diagnostics.[323–326] It was shown that SiF_4/O_2 plasma could significantly strengthen the SiO_xF_y passivation layer. This property gave rise to the so-called STiGer process,[327,328] which alternates SiF_4/O_2 plasma deposition with SF_6 plasma etching. Although the STiGer process does not induce process drift like the Bosch process, the latter is usually preferred by companies to avoid using liquid nitrogen. However, as mentioned in the introduction, today's chillers provide lower and lower temperatures, making them suitable for cryoetching.

Cryogenic processes have also been used to etch other materials, including porous low-K dielectrics such as organo silicate glass films without damaging the material at the sidewall.[19] This second example is illustrated in Fig. 33(b). The key idea is to fill the pores of the materials with a gas (C_4F_8 for instance), by condensation at very low temperatures as it is shown in the inset of Fig. 33(b), in order to reduce PID. A proof of principle was obtained using C_4F_8 molecules mixed with SF_6 at −120 °C.[329] Later, it was shown that a higher boiling point organic such as perfluorotetraglyme ($C_{10}F_{20}O_5$) could be used at a substrate temperature between −55 and −35 °C to fill the pores before the etch step and protect the material from PID.[330] This temperature can be easily reached using conventional cryo-coolers.

Silicon texturation can also be obtained by cryoetching. In SF_6/O_2 plasma standard cryoetching, if the O_2 flow rate is increased, black silicon is easily formed at the surface with the appearance of a kind of grass at the surface of the silicon wafer[331,332] [see Fig. 33(c)]. An overpassivating regime is reached, which leads to a partial etching of the surface and the formation of micromasks at the surface, as schematically illustrated in the inset of Fig. 33(c). Once columnar silicon microstructures have formed, the passivation of the vertical sidewalls is initiated, favoring vertical etching of the self-organized patterns. These textured crystalline

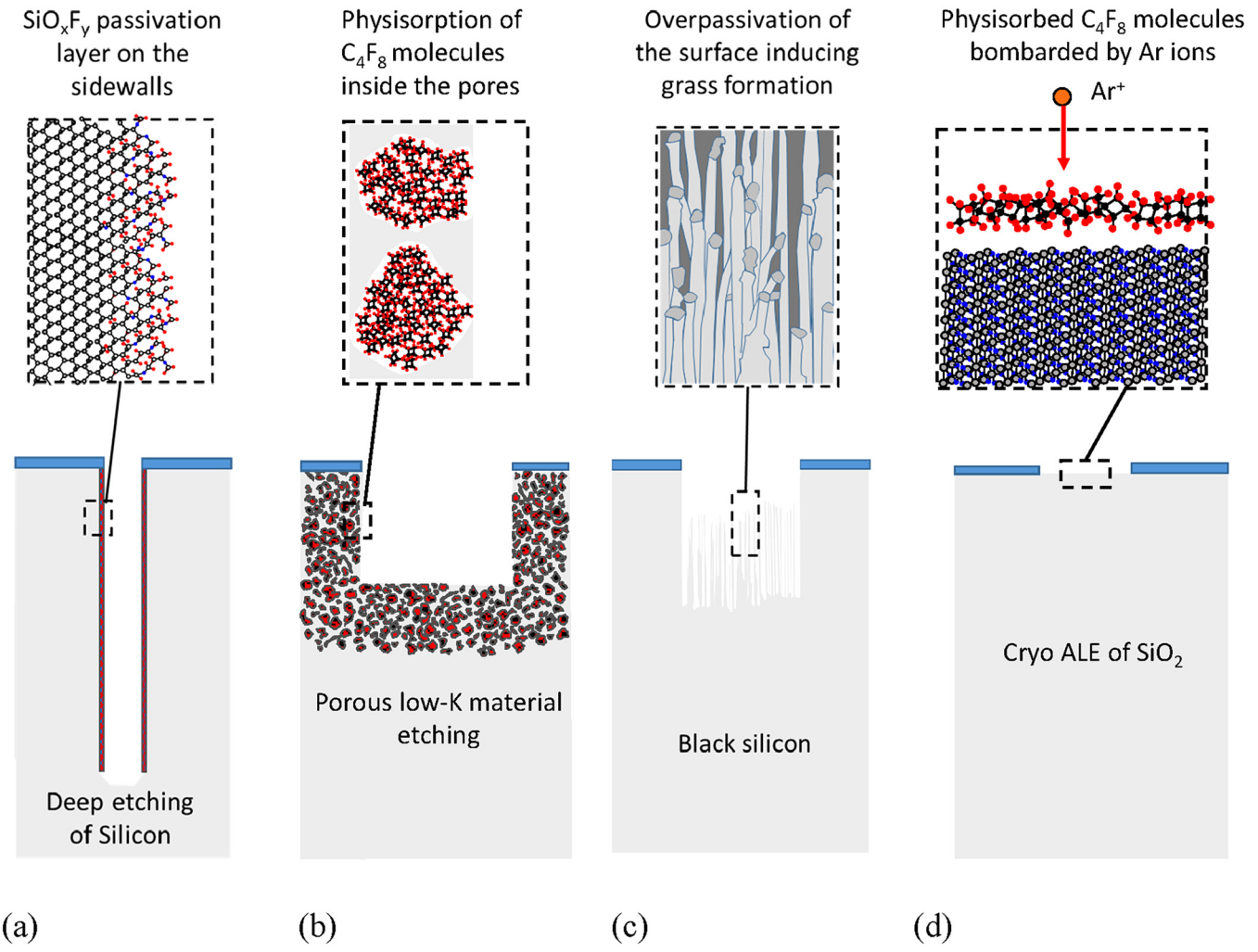

FIG. 33. Schematic of the etched profiles of features obtained for different purposes of cryogenic etching process. (a) Deep etching of silicon. Formation of an SiO_xF_y layer on the sidewalls at low temperatures. (b) Etching of porous low-K materials with a reduced PID by C_4F_8 gas condensation inside the pores at −120 °C. (c) Black silicon formation in overpassivating regime inducing micromasking and forming grass on the silicon surface. (d) Cryo-ALE of SiO_2 by physisorption of molecules at the surface.

silicon surfaces are of interest for solar cell applications[333] or to develop a very large surface area.[334]

Finally, a cryogenic method can be employed for atomic layer etching (cryo-ALE). Some experiments have been carried out on SiO_2.[319,335] The modification step consists in physisorbing C_4F_8 molecules on an SiO_2 surface as represented in Fig. 33(d). Then, the etching step is performed more classically with Ar ion bombardment. CF_x is formed at the surface and interacts with SiO_2. An etch per cycle of about 0.4 nm was achieved using this technique. The process is very stable since no deposition occurs on the reactor walls, which avoids process drift.

These developments are only examples of cryoetching process utilization. Tuning the substrate temperature to low values can significantly modify the etch rate and the etch selectivity.[336] Physisorbed species at low temperatures play an important role as highlighted by several authors.[69,337] It can significantly modify the surface composition as shown in the case of silicon[338] and silicon nitride[339] interacting with SiF_4/O_2 plasma at low temperatures. Reduced diffusion of the species on the surface, physisorption, and longer residence time at low temperatures are very attractive properties that can be used to develop new etch processes.

3. Challenges and roadblocks

Etching tool technological developments are necessary for the deployment of cryoetching processes in industrial production.

Chillers that can operate at very low temperatures are now available and are still evolving toward very low-temperature operation. Chuck temperature uniformity has to be high since small temperature variations can significantly modify the etch profile.

As mentioned in the overview part, particular attention is dedicated to dielectric high-aspect-ratio cryoetching for which selectivity is sometimes wanted, but sometimes not. Metals can also be successfully etched using cryoetching as in the case of molybdenum nanopillar microfabrication.[340]

The mechanisms involved such as physisorption, species diffusion and transport at the surface, formation of stable molecules at very low temperatures, and change of the layer composition by cooling the substrate have to be further studied and better understood to control cryoetching processes. In particular, there is a trade-off between surface diffusion of physisorbed species, which is reduced at low temperatures and their residence time at the surface, which increases when lowering temperature. X-ray photoelectron spectroscopy (XPS)—after the plasma process—and attenuated total reflectance-Fourier transform infrared (FTIR) spectroscopy (*in situ*) are worthwhile characterization techniques to analyze the surfaces at low temperatures.

Modeling has to be developed taking into account surface cooling. Molecular dynamics[337] and density-functional theory[341] can provide very valuable information on the mechanisms and understanding. Monte Carlo methods can also be used to simulate profiles.[342] Predictive profiles can be provided especially if delayed desorption of physisorbed species can be integrated in the code as suggested by Rudenko *et al.*[343]

4. High-aspect-ratio etching of silicon oxide and nitride stacked layers applied to 3D-NAND flash memories

A significant advance was reported recently on high-aspect-ratio dielectric cryoetching.[11] This process development is dedicated to 3D-NAND flash memory microfabrication. In such devices, a large number of SiO_2 and Si_3N_4 layers are alternatively stacked (ONON) and need to be etched with a low selectivity. It is well known that SiO_2 is efficiently etched by aqueous HF solution.[344] In 1992, it was reported that the etch rate of SiO_2 by CHF_3 plasma could be significantly enhanced by lowering the temperature to about −50 °C.[345]

A plasma process involving HF, H_2O, and PF_3 gases was successfully used to etch very high aspect ratio of ONON holes at a substrate temperature as low as −70 °C as shown in Figs. 34(a)–34(c). H_2O and HF molecules are very volatile at low pressure. But co-adsorption of HF and H_2O molecules is enhanced at low

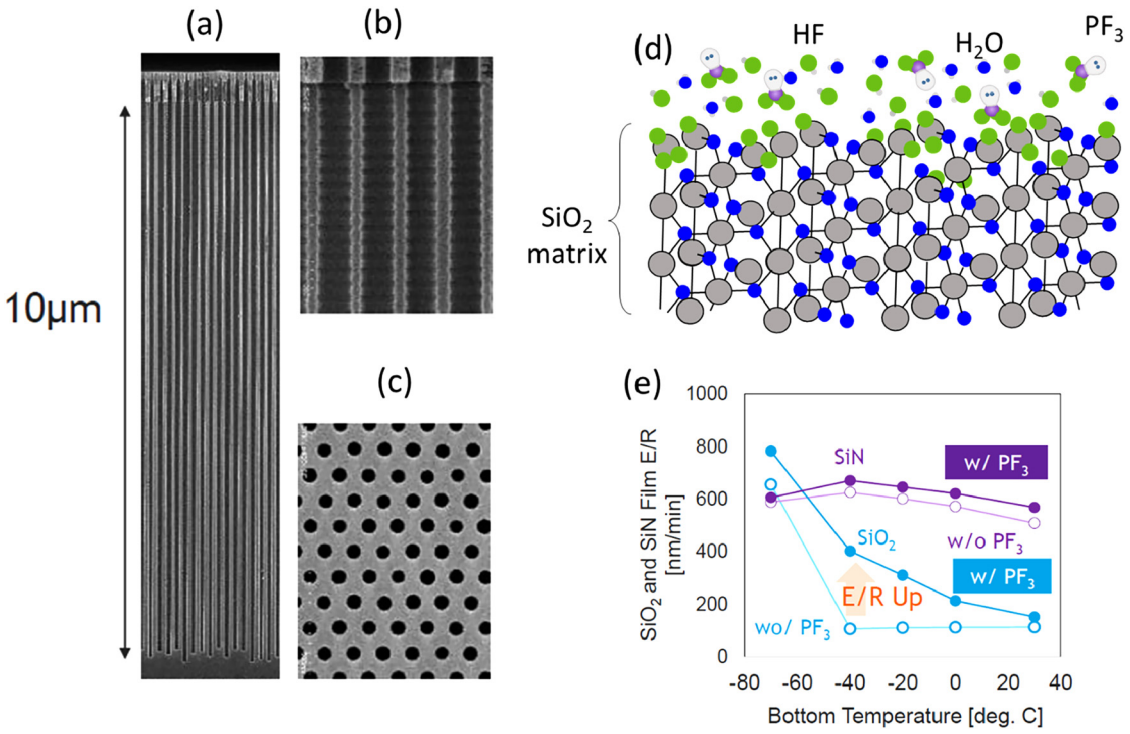

FIG. 34. Cryoetching for 3D-NAND flash memories. (a) SEM images of 100 nm diameter 10 μm deep holes etched through a stack of more than 400 oxide and nitride layers using a cryogenic etch process involving HF, H_2O and PF_3. (b) Zoom of the etched holes below the mask. (c) Top view of the etched holes cut at bottom by FIB. (d) Schematic of the chemical mechanism at the SiO_2 surface. (e) Si_3N_4 and SiO_2 etch rate vs temperature with or without PF_3 in the plasma mixture [(a), (c), and (e): Reprinted with permission from Kihara *et al.*, in *2023 IEEE Symposium on VLSI Technology and Circuits* (The Japan Society of Applied Physics, 2023), pp. T3-2. Copyright 2023, The Japan Society of Applied Physics].

temperatures and can react with SiO_2 and Si_3N_4 under ion bombardment. It was shown that P containing gases can also improve the adsorption of water and lower the energy for fluoridization as illustrated in Fig. 34(d). The etch rate of SiO_2 and Si_3N_4 is plotted versus temperature in Fig. 34(c). SiO_2 etch rate increases when the substrate temperature decreases. It reaches the Si_3N_4 etch rate value at −70 °C. By adding PF_3 gas in the plasma mixture, the etch rate of both materials is higher. The growth of a passivation layer prevents the sidewall from lateral etching. Using this process, 10 μm deep holes with 100 nm diameter were etched over 400 oxide and nitride layers.

It is worth noting that this new process does not use gases with a high GWP as compared to conventional processes. Besides, this process avoids mask necking that can induce lower etch rate and defects on sidewalls. This new process is expected to be adopted for HVM.

It is also considered to utilize this new process for other etching applications as well. Meanwhile, the co-adsorption phenomenon at the surface has to be further studied to better understand the etching mechanism at low temperatures. The surface electric conductivity of the deposited layer is also enhanced in cryoetching as recently reported by Hsiao *et al.*,[346] which can avoid charging buildup, ion trajectory deviation resulting in the appearance of defects such as "bowing effect."

5. Outlook

Plasma etching tools will likely require hardware modifications to make them more suitable for cryoetching. The temperature at the wafer surface has to be highly uniform. The control of the surface real temperature is also a key issue. Usually, only the setpoint temperature of the chuck is provided, but the surface temperature, which may vary significantly under plasma exposure and especially by a high-energy ion flux, remains difficult to measure. Improvement of heat resistance reduction at the pedestal is also continuously needed from the view of energy saving and efficiency.

Although very few works have been reported so far, cryoetching of metallic materials is also of interest and under investigation, especially using a cryo-atomic layer etching process.

It is now accepted that cryogenic etching offers new prospects in nanofabrication and will play an important role in the development of next component technology.

N. New diagnostics, metrology, and real-time control in semiconductor plasma etching

Masaru Hori, Makoto Sekine

1. Status and promising developments

In the history of plasma etching research and development,[2,347] a major obstacle to improving the accuracy of the etching process has been the lack of suitable diagnostic and measurement techniques for particles in plasmas.[348] To address this issue, laser-induced fluorescence spectroscopy, absorption spectroscopy, appearance potential mass spectrometry, and cavity ring-down methods were introduced to clarify the density and behavior of radicals in the gas phase.[349] As wafer diameters became larger, higher-density plasma processes were introduced, thus requiring precise control of the dissociation process for gases and of the electron temperature. Eventually, the need to determine not only the density of electrons but also their energy distribution led to the introduction of techniques such as surface-wave probes, laser Thomson scattering, and emission spectroscopy, in addition to conventional Langmuir probes. In these methods, noble gases are introduced as tracers to evaluate the electron energy distribution. Furthermore, as a method to control the density and energy of ions and radicals, pulsed plasma technology has been used, in which pulsed power is applied to the plasma source and substrate.[185] Measurement of the time-evolution of particle dynamics is also becoming increasingly important.

As discussed in Secs. II D and II O, the use of AI has in recent years added various impacts on etching process optimization, process control,[60,193] simulation, and acquisition of fundamental data sets.[238] In particular, in emission spectroscopy (OES), it is almost the only monitoring method that has been employed as etch endpoint detection[217] in mass production etch systems since the 1970s. This is because OES reliably provides real-time information on plasma chemistry during etching without invading the plasma. Starting with early applications of OES, such as the analysis of process parameters as "chamber fingerprints" in etch systems using neural networks,[219] AI has great potential to enhance OES and other monitoring technologies, as seen in recent rapid developments.

In addition to measurement and control of particle behavior in the gas phase, measurement techniques for surface reactions have been developed to gain insights into the nonequilibrium physicochemical reaction field induced in the material to be etched by the interaction of radicals and ions. Spectroscopic measurement techniques, such as XPS, FTIR spectroscopy, and spectroscopic ellipsometry, in addition to atomic-scale microscopy, have been used to investigate surface chemical bonding and surface film structures after plasma etching. To meet the requirements for real-time or *in situ* measurements, it is necessary to integrate such instruments into modern plasma etching systems. The gas-phase and surface reactions associated with particles in different plasma processes have been summarized.[349] This section describes new diagnostics, measurement, and real-time process control methods that have been developed based on data obtained for etching processes and discusses their future potential for plasma etching.

2. Challenges and roadblocks

To form high-aspect-ratio holes, such as those required for the fabrication of 3D memory devices, plasma etching using fluorocarbon gas is generally used because it can achieve a high etching selectivity ratio for SiO_2, SiN, Si, and organic resists. The core of this chemistry lies in the nonequilibrium physicochemical reactions induced among fluorocarbon radicals, ions, and the material to be etched. It is particularly important to control the intermediate layer formed on the surface of the material during etching. Chemical analysis techniques such as angle-resolved XPS have been used to analyze this layer, but the behavior of the etchant and etching reaction products, which are formed simultaneously in the interlayer, has not yet been fully elucidated.

Recently, Ohya *et al.*[350] employed time-of-flight secondary ion mass spectrometry using C_{60}^{2+} ions to investigate the microscopic behavior of reaction products in the intermediate layer (<2 nm thickness) formed during SiO_2 etching by a fluorocarbon and oxygen mixed gas plasma, and new findings were obtained, as shown in Fig. 35.[350] In Region I, the fluorocarbon film is thick enough to prevent ions directly reaching the SiO_2 surface. Nevertheless, etching of SiO_2 still occurs in this region, suggesting that high-energy ions in the plasma impart kinetic energy to the atoms in the fluorocarbon layer, releasing etchants such as F that cause chemical mixing at the interface and forming an SiOF intermediate layer. Etching proceeds even in the region where ions do not reach SiO_2, suggesting that high-energy ions give kinetic energy to the fluorocarbon layer and the etchants such as F supplied from the fluorocarbon film promote chemical mixing and the formation of the SiOF intermediate layer. Desorption of etching reaction products is thought to occur through the SiOF and fluorocarbon layers. However, as the oxygen content becomes higher, the thickness of the fluorocarbon film decreases and the etch rate increases as the SiOF layer on SiO_2 becomes thicker due to ion impact. Therefore, the etch rate strongly depends on the thicknesses of both the fluorocarbon and SiOF layers (between Regions I and II). As the oxygen content further increases, direct reaction between the ions and the SiOF layer occurs and the thickness of this layer decreases, causing the etch rate to saturate in Region II. These results quantitatively reveal that the etching properties of SiO_2 are strongly related to the presence of SiOF as an intermediate layer. This provides valuable information for predicting the etching properties of SiO_2 and other materials and for further development of HAR etching methods.

Atomic layer etching has attracted attention as a method for forming precise 3D micropatterned structures, and many *in situ* measurement techniques have already been used to analyze surface reactions. In particular, layer-by-layer etching of 2D thin-film materials, such as graphene, MoS_2, and WS_2, without damage to the underlying material is becoming increasingly important. Recently, a method has been reported that enables *in situ* observation of etching of 2D materials by TEM.[351] Figure 36 shows the experimental setup and results for layer-by-layer etching of graphene by oxygen radicals obtained using electron energy loss spectroscopy. This allows us to understand how graphene is etched by oxygen radicals at the atomic layer level. Furthermore, TEM reveals that the graphene etch rate varies with location, and increases in the order of planes < edges < defects. This measurement technique enables real-time observation of the microscopic dynamics of plasma-induced surface reactions.

The above diagnostic and measurement methods are expected to allow not only ultrahigh-precision plasma etching but also to contribute to the advancement of low-temperature plasma science. Currently, etching characteristics, such as the etch rate, pattern profile, and etching selectivity, are described in terms of external parameters (equipment parameters), such as gas pressure, flow rate,

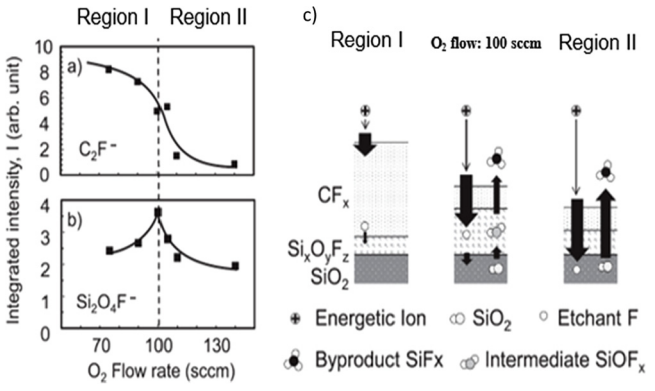

FIG. 35. Integrated intensities over the entire depth ranges of (a) C_2F^- and (b) $Si_2O_4F^-$ as a function of O_2 flow rate. (c) Schematic of the model for the dominant rate-limiting step of SiO_2 etching of each region.

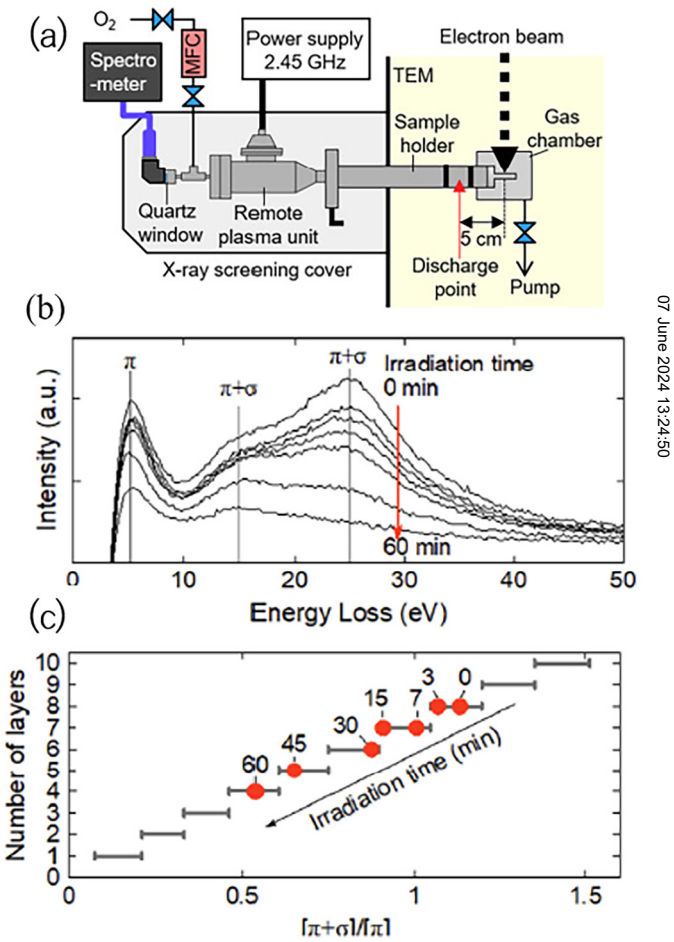

FIG. 36. Graphene etching process observed *in situ* by TEM and EELS. (a) Experimental setup for *in situ* TEM and plasma source. (b) Plasmon peaks of EEL spectra in low-loss region after background subtraction. (c) Relationship between number of layers and $[\pi + \sigma]/[\pi]$ measured in the present experiment for remote oxygen plasma irradiation.

and RF power. However, these parameters are not universal in the sense that they depend on the equipment being used. By describing etching properties in terms of particle parameters (internal parameters) that directly contribute to the etching reaction, a reliable and universal dataset can be constructed. We refer to this as an evaluated and authorized dataset. To realize data-driven processes, referred to as plasma informatics, combining AI and an integrated database of eADSets will make it possible to identify the active species that play important roles in plasma processes, elucidate the structure of interlayers that determine surface reactions, and construct a time-evolving recipe to continuously control the etching process as it progresses. In the future, AI-controlled, science-based tailor-made etching processes will become possible using autonomous plasma-based fabrication systems.[349] Such an approach is expected not only to realize ultrahigh-precision plasma etching but also to create a paradigm shift from trial-and-error development to science-based development. It will also be helpful for the realization of green plasma etching processes with ultralow energy consumption.

O. Machine learning for scale-bridging modeling of plasma etch

Shoubhanik Nath, Ali Mesbah

1. Overview and open challenges

With micro- and nanoelectronics fabrication moving toward ever smaller critical dimensions, it has become increasingly crucial to understand the foundational atomic-scale processes at the heart of plasma etch. These processes are governed by plasma-surface interactions, which are inherently multiscale and can span a vast range of length and time scales from Angstroms to meters and picoseconds to seconds, respectively.[352,353] Modeling of the three overarching scales—atomic (microscopic), mesoscopic, and macroscopic—has been investigated in isolation, with different techniques for each. Atomic processes are commonly studied with DFT or with *ab initio* molecular dynamics (AIMD). The mesoscopic behavior is investigated using MD simulations, possibly with coarse-grained (CG) fields and structures, or even with Monte Carlo simulations. Finally, the macroscopic scale warrants a continuum description with rate equations. However, to establish a foundational understanding of plasma etch, it is imperative to combine these disparate scales in a unified multiscale modeling framework that connects global process parameters to atomic interactions at the plasma-solid interface. Such scale-bridging plasma etch models can create unprecedented opportunities for investigating new chemistries and substrate materials *in silico* as well as for precise etch control. These advances can, in turn, play a transformative role toward developing more sustainable plasma etch processes and realizing increasingly smaller critical dimensions with improved uniformity and decreased defects, essential for the fabrication of next-generation micro- and nanoelectronic devices.

In recent years, ML has made an enormous impact in many scientific disciplines, including in the field of low-temperature plasmas[238,354] and plasma-assisted processing in the semiconductor industry.[355] In particular, ML has received growing attention for modeling and simulation of plasma physics, plasma chemistry, and plasma-surface interactions, as comprehensively surveyed recently.[356] However, ML-assisted modeling of plasma-surface interactions in plasma etch is largely underexplored. Toward establishing scale-bridging models for plasma etch, ML can play a critical role in three distinct areas: (i) approximating the quantum interactions between plasma species and surface to enable investigation of plasma-induced surface effects via molecular dynamics for new etch chemistries; (ii) extending MD simulations to longer times to enable describing surface processes that give rise to the physics observed at the reactor level; and (iii) connecting the microscopic evolution of surface to macroscopic descriptions of plasma to enable systematic investigations of plasma-induced surface effects, such as the formation of surface roughness and defects, in relation to plasma processing conditions. The state-of-the-art in ML in each of these areas, along with perspectives as to how these ML advances can transform the modeling and simulation of plasma etch processes, are discussed below.

2. Machine-learned interatomic potentials

One of the primary barriers to accurately represent atomistic interactions in MD is the availability of suitable interatomic potentials.[357] While various semiempirical interatomic potentials have been used for Si etching with varying degrees of accuracy,[358,359] creating interatomic potentials for new plasma etch chemistries is challenging and nonintuitive. To this end, machine-learned potentials (MLPs)[360–362] can greatly facilitate MD investigations of novel etch chemistries for which foundational knowledge is lacking and interatomic potentials do not exist. The main idea in MLP is to leverage a database of structures, whose energies, forces, and stresses are obtained from DFT calculations, in order to learn a data-driven representation for interatomic force fields by mapping structure properties onto approximate atomic descriptors (e.g., positions, bond angles).[363] This representation must be invariant to translation, rotation, and permutation of atoms; that is, MLP should have built-in symmetries. The two common types of MLP are neural networks, e.g., Behler–Parinello neural networks,[242] and kernel-based models, e.g., kernel-based Gaussian approximation potentials.[364] Behler–Parinello neural networks were a landmark development wherein inputs to the MLP are symmetry functions that are dependent on the local environment of an atom and are invariant to rotation and translation. Gaussian approximation potentials, on the other hand, also rely on symmetry functions *in lieu* of atomic coordinates but use nonparametric Gaussian process regression that can generally have more favorable data efficiency than neural networks for approximating interatomic force fields. Since a key challenge in learning MLP is often lack of adequate data from expensive DFT calculations, incorporating physics knowledge, for example, analytical knowledge of bond-order potentials,[365] can improve the data efficiency, as well as the generalizability of MLP. Another major recent development that can become useful for plasma etch is general-purpose tools like DeePMD (Ref. 368) that allow for the creation of an end-to-end pipeline for deep learning of interatomic potentials directly from AIMD simulations.

Nonetheless, an important barrier to the adoption of MLP in plasma etch can stem from the need for rich and large DFT datasets. Using graph neural networks to represent atomic structures holds promise for enhancing data efficiency by naturally encoding invariances and system geometries (e.g., interatomic distances, bond angles) in the MLP architecture.[367] Additionally, the computational cost of graph neural networks is shown to scale linearly with the system size,[368] which can be especially useful for MD simulation of plasma etch systems consisting of many species. A promising avenue toward increasing data efficiency for learning MLP and improving their accuracy is the use of ML-guided optimal sample selection and active learning methods[369] to iteratively query the design space of molecular structures in DFT calculations in a systematic and resource-efficient way. One key advantage of active learning is that it naturally quantifies the uncertainty in the model and provides a clear indication of the regions of applicability of the MLP. A graph neural network-based MLP with iterative optimal search will not only encode the structure of the molecule in question but also require significantly less data to arrive at accurate interatomic potentials.

3. ML for coarse-graining molecular dynamics

While MLP can provide high accuracy in calculating potentials for MD simulations, these potentials are computed from all-atom interactions and, thus, the simulation times can become severely limited by the size of the system. Coarse-graining has become a widely used approach to extend the length and time scales of MD simulations and investigate how molecular-scale effects can influence continuum-level physics,[370] even though it is largely unexplored in plasma etch, with works done mostly on organic semiconductors.[371,372] Further, MD simulations of plasma etch mostly rely on a limited number of atoms (few thousands) and only up to a simulation time of a few picoseconds,[373] whereas experimental plasma etch cycle times can be on the order of tens of seconds. CG molecular dynamics can be advantageous for enabling longer simulation times to better represent the relaxation processes that occur in the bulk substrate during ion bombardment.

Coarse-graining involves clustering groups of atoms into a single bead, defining coordinates for these beads (i.e., coarse-grained coordinates), and fitting force-field approximations that interpolate interactions between them. Unsupervised and supervised learning plays an important role in learning CG coordinates and force fields using all-atom MD data.[374,375] However, ML-assisted coarse-graining commonly relies on a predefined set of CG coordinates. Yet, unlike, for example, coarse-graining of proteins that have well-defined structures,[376] in a lattice model for etch substrates, identifying strongly related atoms that are clustered in a CG bead to define CG coordinates can be a major hurdle. This is especially the case if the lattice becomes increasingly amorphous as etch progresses, making it nonintuitive to define CG beads. An open problem of significant importance for CG molecular dynamics of plasma etch systems is how unsupervised learning can be intimately coupled with supervised learning to unify the identification of appropriate CG coordinates for etched surface with the approximation of CG force fields. Generative models such as variational auto-encoders,[377] a deep learning strategy for unsupervised learning of uncertain distributions, can be particularly useful for learning CG representations of atomistic descriptions with unknown distributions (see Fig. 37). Coupling (deep) neural network models of CG force fields with generative unsupervised learning will aid in retaining the atomistic information that is otherwise lost during coarse-graining by traditional means with predefined

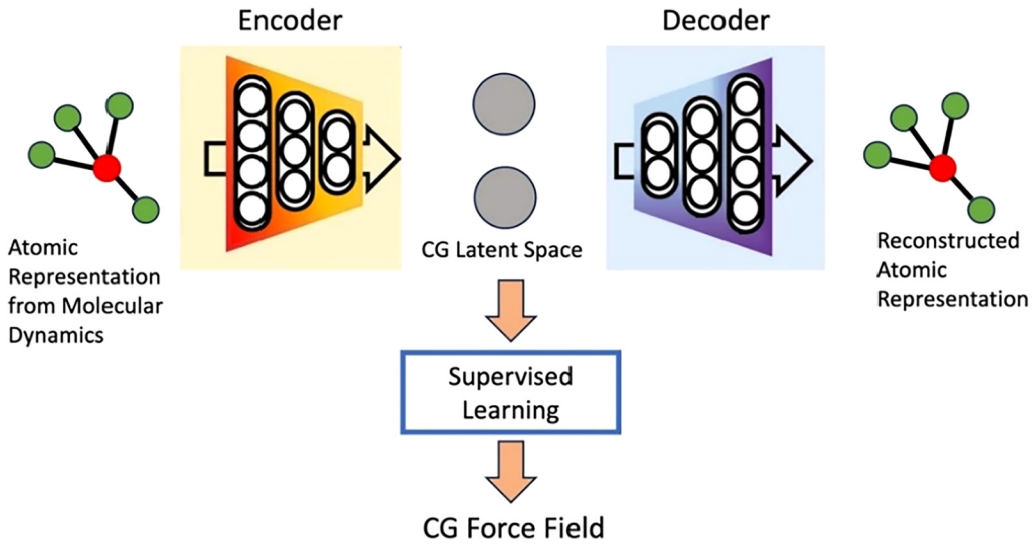

FIG. 37. Architecture of generative variational autoencoder to coarse grain atomic data. Atomic data are encoded onto a low-dimensional CG latent space. The decoder is trained to reconstruct the CG data back to high-dimensional atomic data. The latent space, representing the space of CG coordinates, is mapped onto a CG force field, which can then be used for molecular dynamics.

coordinates.[378] Such ML-assisted approaches to CG molecular dynamics can create unprecedented opportunities for developing novel insights into plasma etch at the mesoscopic scale.

4. Outlook

Emergent physics can only be observed when MD simulations are performed on a large number of particles, which can quickly become computationally intractable. While coarse-grained MD can extend the length and time scales of simulation, it does not generate macroscopic surface kinetic models that describe the evolution of the surface and surface species. When coupled with models for bulk plasma and sheath, surface kinetic models can describe the time-evolution of key process variables in plasma etch such as etch profile, feature profile, surface roughness, critical dimension uniformity, and defect formation. Hence, a scale-bridging model of the plasma-solid interface that connects *ab initio* calculations to surface kinetics through (coarse-grained) molecular dynamics can pave the way for describing fundamental surface processes in relation to reactor-level plasma process inputs (see Sec. II P). However, multiscale models of plasma etch, connecting the surface to bulk plasma, are mostly based on surface Monte Carlo models,[379–381] which may not provide a detailed picture of the surface processes at an atomistic level.

While there have been a few recent works on surrogate modeling of plasma-surface interactions in sputtering,[356] Ml-assisted scale-bridging modeling of surface processes from first principles is largely an unexplored area of research in plasma etch. ML can be particularly useful in scale-bridging efforts to approximate physics from preceding scales, especially in the presence of complicated and numerous interactions, where semianalytical methods might be too cumbersome. As depicted in Fig. 38, such a scale-bridging model can include the following salient steps: (i) learning interatomic potentials from *ab initio* data, with active learning for efficient exploration of the design space of molecular structures; (ii) learning coarse-grained coordinates and force fields to extend the length and time scale of molecular dynamics; and (iii) learning states occupied by different species on the surface, as well as their associated transitions, from (coarse-grained) molecular dynamics, which can then generate a set of Master equations describing surface processes. With such Master equations, one can either run kinetic Monte Carlo simulations to evolve the surface and investigate the dynamics of the plasma-solid interface when coupled with accurate plasma models. Such a scale-bridging paradigm for modeling plasma-surface interactions in plasma etch will encode atomistic phenomena that govern macroscopic physics and, hence, can enable exquisite control of

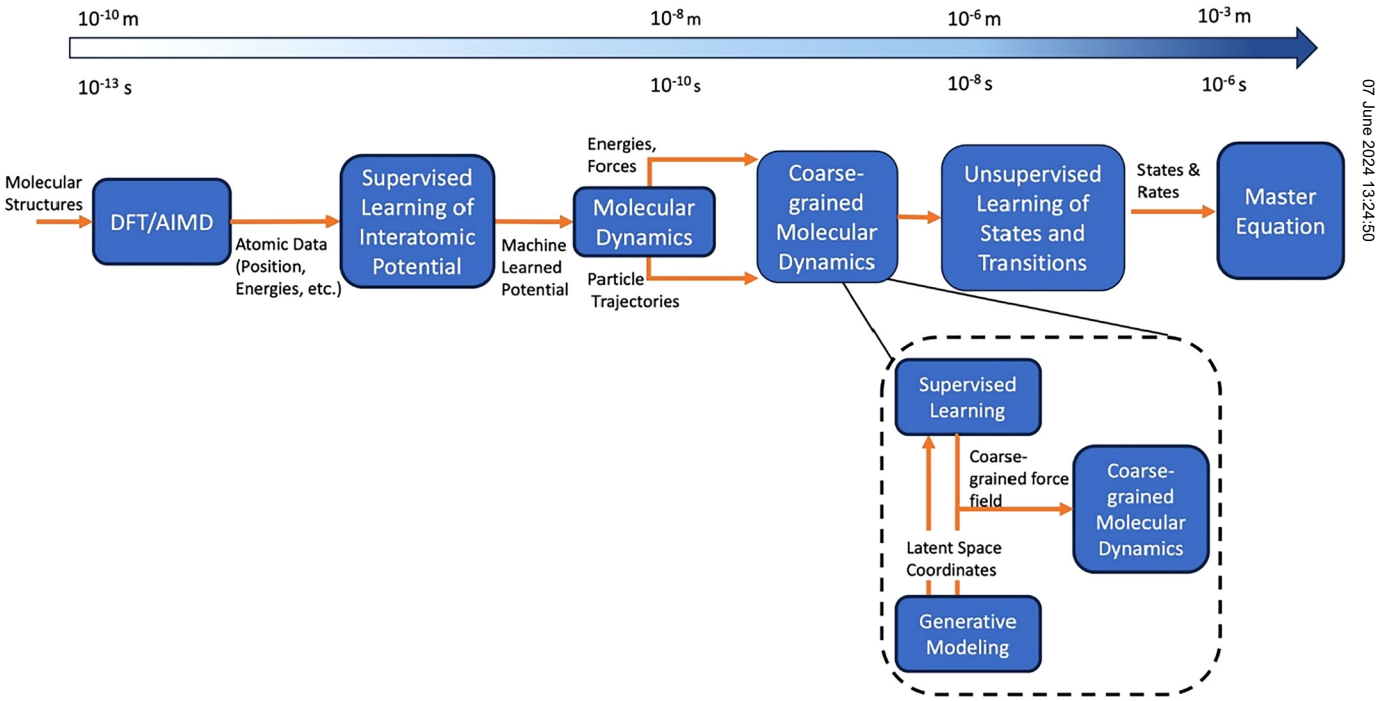

FIG. 38. Perspective on machine learning-assisted scale-bridging modeling of plasma-surface interactions. Molecular structures are fed to DFT calculations, or *ab initio* molecular dynamics, to generate atomic data, which is then used to learn interatomic potentials. These potentials can be used in molecular dynamics to generate atomic trajectories, which, in turn, can be used to learn coarse-grained latent space of molecular dynamics. Along with energies and forces, the coarse-grained latent space enables establishing coarse-grained force fields, which can drive coarse-grained molecular dynamics over longer time- and length-scale. Outputs from these simulations will inform transition states and probabilities for surface processes. Such a scale-bridging modeling paradigm will enable the creation of surface kinetic models that capture atomic information.

atomic-scale surface processes toward the fabrication of the next-generation memory and logic devices.

This section focuses on the fundamental modeling of plasma etch. Additionally, there are ample emerging applications of ML for process development and design, process optimization and efficiency enhancement, and real-time process monitoring and control of plasma-assisted semiconductor fabrication, as discussed in a recent survey.[355] The application of ML for so-called equipment intelligence and smart manufacturing of micro- and nanoelectronic devices is an emerging area of research and has already drawn significant interest from the semiconductor industry. Notable recent examples include the predictive decision-making capabilities offered by digital twins and the AI-enabled human-machine collaboration toward etch recipe design.[193] Such advances can offer otherwise unattainable insights into process intricacies and significantly impact the time-to-market of new processes and products and the drive for greater productivity and yield.

P. Reactor and feature-scale computational modeling

Nobuyuki Kuboi, Mark J. Kushner

Plasma etching processes continue to become more complex with the introduction of new materials and three-dimensional device architectures[382] having extreme aspect ratios (AR)[383] or having atomic layer requirements.[384] These processes are conducted with new plasma sources, many using pulsing[385] and multiple frequencies.[386] With the cost of developing such reactors and processes continuing to escalate, there is increasing reliance on and greater expectations for computational modeling to speed reactor design and process development. In this regard, there are two components of modeling—reactor scale and feature scale. In equipment design, reactor scale models have the goal of representing power coupling to the plasma, plasma transport and chemistry, and radiation transport and plasma-surface interactions (wafer and reactor walls), all of which are optimized to minimize power consumption and to deliver uniform reactive fluxes to the wafer. Feature-scale models use the energy and angular distributions of those reactive fluxes to the wafer to predict the evolution of on wafer features, having scale lengths from atomic layers to many micrometers.

1. Reactor scale modeling

There are several high level expectations for reactor scale modeling. The first is investigation of fundamental plasma transport and plasma chemical reactions, and their interactions with plasma bounding surfaces.[387] The second is extension of that capability to *clean-sheet* design of new plasma reactors and to improving designs of current systems, including process design. The next expectation is the production of vast amounts of computational results that are used as training data for ML approaches to equipment design, process development, and real time control.[388] At the highest level is the development of digital twins of plasma equipment that track the state of the reactor and are able to predict, for example, process drift or the need for preventative maintenance.[60]

As one progresses from fundamental studies to the digital twin, the code requirements also change. Fundamental studies likely require kinetic approaches to plasma and neutral transport.[389–392] Although highly capable, by their nature, kinetic simulations are computationally intensive and so may be limited in their dimensionality, plasma density, number of species, ability to address fluid dynamics, and length of calculation. The latter issue is important when considering, for example, pulsed systems and plasma wall interactions where simulations must address several pulsed periods and gas residence times, and as much as a minute for surfaces to be passivated. Considerable progress has been made in addressing these needs using continuum[393–395] and hybrid techniques,[68,396,397] models, which enable these capabilities by making approximations at the kinetic level (see Fig. 39). *Clean-sheet*-capable models require three-dimensional compatibility with established computer-aided-design

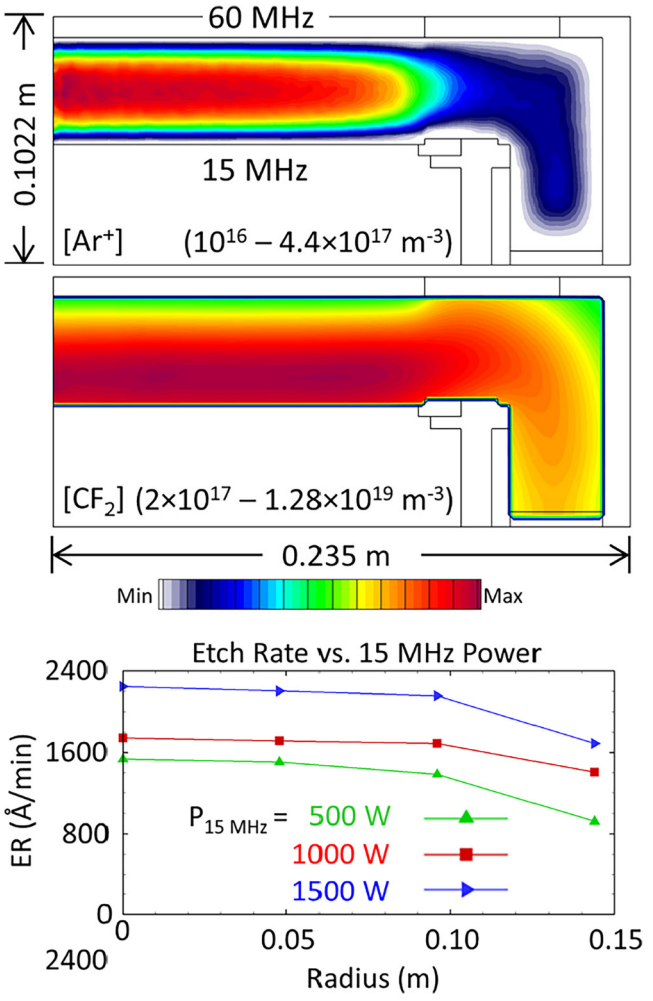

FIG. 39. Predictions for ion and radical densities, and SiO_2 etch rate from a 2D hybrid model. Reactor is a two-frequency (15, 60 MHz) capacitively coupled plasma sustained in $Ar/C_4F_8/O_2$ gas mixtures. Reprinted with permission from Shahid Rauf and Ajit Balakrishna, J. Vac. Sci. Technol. A **35**, 021308 (2016). Copyright 2016, American Vacuum Society (Ref. 398).

programs, integrated with plasma-surface chemistry, radiation transport, nonlocal electromagnetics, and circuit models, which provide the interface between power delivered from the supply to voltage applied to the electrodes. The digital twin model additionally requires capabilities to assess wear-and-tear on the physical properties of the reactor, for example, erosion of plasma-facing materials and changes in positioning and tolerances of parts during preventative maintenance. The computational generation of ML datasets needs rapidly executing models in order to run tens-of-thousands of cases over a large dynamic range, likely using cloud resources.

To make progress in this continuum of modeling requirements, from fundamental modeling to digital twins, it is necessary to acknowledge the strengths and weaknesses of different modeling approaches. In the near term, kinetics codes that excel in fundamental studies will likely not meet the requirements for clean-sheet design of reactors using complex chemistry and high plasma densities. Fluid based codes, which may have the speed and capability for multispecies and surface chemistry needed for clean-sheet design and digital twins, lack the ability to comprehensively address kinetic process, kinetic driven plasmas instabilities, and nonlocal transport. Hybrid codes lie somewhere in-between. Acknowledging that one modeling technique will likely not span the required parameter space, a method for linking and leveraging results produced by the different modeling techniques will be required.

Underlying all reactor scale models is the need for a robust database of fundamental reactions, electron-impact cross sections, surface reaction probabilities, and reaction mechanisms for process relevant chemistries. The need for completeness and precision of the data and reaction mechanisms also varies from fundamental studies, which can be performed with a few species, to process design and digital twins that require comprehensive reaction mechanisms for multicomponent molecular gas mixtures. Given the rapid progress in the development of models using kinetic, fluid, and hybrid techniques, there is high confidence that the needed plasma physics will be available in models for clean-sheet and digital twin approaches. At that point, the rate-limiting step is the availability of reaction mechanisms for process relevant gas mixtures. In fact, the models that are now available are already limited in their ability to aid in process design by the lack of fundamental data for gas-phase and surface processes. There has been a decades-long underinvestment in development of fundamental data and reaction mechanisms. That said, there has been considerable progress in collating and validating process relevant reaction mechanisms[398] and development of ML methods to predict fundamental reaction data.[399] A systematic and collaborative effort is needed to generate those data and mechanisms for reactor and feature-scale modeling to meet the objectives discussed here.[400]

2. Feature-scale modeling

The modeling and simulation of feature-scale profiles for plasma etching of Si, SiO_2, SiN, metal/metal oxide, and organic/low-k films using methods, such as string,[401,402] shock-tracking,[403,404] level-set,[174,405] and cell removable (or voxel)[68,406–408] methods in two- or three-dimensions have been actively developed since the 1980s. Models are now able to not only address feature-scale profiles but also assess damage distributions induced by high-energy particles using a slab model in conjunction with the voxel method.[409] These models have been used to gain insights into the mechanisms and control of continuous wave, pulsed, cyclic, cryogenic, and atomic layer etching of structures including trenches, high-aspect-ratio contacts (HARC), SAC, and gate sidewalls of planar and FinFET (see Fig. 40). Due to the recent and rapid improvement in central processing units, graphical processing unit, and parallel algorithms, models have been developed in conjunction with direct molecular dynamics simulations[236] and a surrogate model as a type of machine learning[410] and used to predict feature-scale profiles. With radical fluxes, and ion energy and angular distributions derived from reactor scale simulations of capacitively coupled plasmas and inductively coupled plasmas,[209] or experimental datasets, variation of feature-scale profiles and damage can be accurately predicted at the wafer level, leading to the optimization of process conditions and chamber maintenance schedules for high-volume manufacturing.

Plasma etching proceeds through symbiotic and coexisting material removal and addition processes. As such, profile simulations for plasma etching must be capable of addressing both material removal (etching) and addition (deposition) processes. This is particularly important in the profile simulation of integrated processes. As with the plasma etching models, string models have been

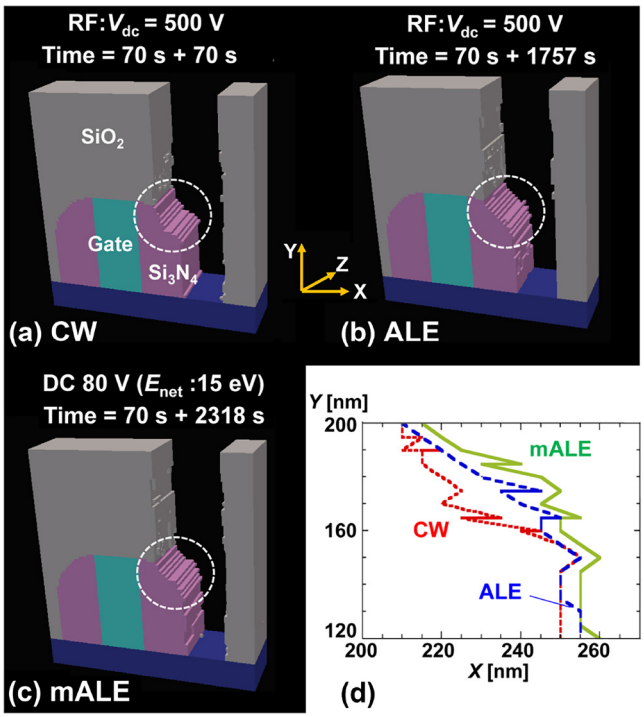

FIG. 40. Simulated feature-scale profiles for SAC etching for (a) continuous wave (CW) processing, (b) realistic ALE, and (c) ideal ALE after performing CW etching of 70 s. (d) Differences in profiles using these methods. Reprinted with permission from Kuboi *et al.*, J. Vac. Sci. Technol. A **37**, 051004 (2019). Copyright 2019, American Vacuum Society (Ref. 412).

used since the 1990s for modeling feature-scale profiles (step coverage) in CVD and PVD.[411,412] More accurate models were later developed using shock-tracking, level-set, and cell removable (or voxel) algorithms for the deposition of Si, SiO_2, SiN, SiC, and metals (W, Ti, Al, Mo, Cr, Cu, TiN).[413–417] These models were mainly used to predict coverage in trench and hole structures and their process dependence for ALD as well as CVD and PVD. Predictions of film properties, such as binding, density, permeability, and adhesion, which reflect the base structure and interface state, are now required as materials such as poly-Si, SiO_2, SiN, SiON, and metals are stacked with organic films in new devices where low-temperature processes (<100 °C) are used. The theoretical aspects of surface reactions and how to achieve good coverage and film properties at low temperatures have not yet been fully investigated. A model that can simulate both coverage and distributions of film properties on a large scale for HARC patterns and complex structures was recently developed using a multiscale algorithm and a statistical ensemble method.[418] These properties are then starting conditions for subsequent etch steps, needed for integrated feature scaling modeling. These deposition models emphasize the importance of controlling gas conditions (composition, degree of dissociation, and distribution), precursor feed time, and surface migration.

Advanced CMOS devices require precise microfabrication in etching and deposition processes for different AR patterns. Prediction and control of feature-scale profiles, damage distributions, and film properties are crucial. Feature-scale simulations have been developed to understand physical and chemical phenomena during etching and deposition processes to predict profiles and determine important factors for process and pattern layout design. Moving forward, simulation technologies will be used for the emerging field of "process informatics" in which the results of real-time predictions are combined with equipped engineering system data, fault detection and classification data, and plasma monitoring data such as OES. These combined data enable process control to ensure that the profile meets the specifications for a semiconductor device fabrication line.[388] To achieve process informatics, it is first necessary to improve profile simulations that are consistent with accurate measurements of the basic plasma properties. After that, improvements in calculation speed are needed so that execution time is comparable to the real process time. Currently, ML,[419,420] fusion physical model with ML,[421] and surrogate models[422] are used to address this challenge. Advances in both physical understanding and computations will lead to real-time process correction at the atomic scale and the realization of the complete digital twin.

III. CONCLUSION

We have discussed the challenges and opportunities for the dynamic period of change that lies ahead for plasma etching and with microelectronics processing in general. In addressing these issues, the views of experts on the topics that will shape plasma etching of the future were shared. These overviews of status, needs, and opportunities provide introductions to topics and literature for new and experienced investigators in the field. The most significant challenges facing plasma etching include addressing both societal and environmental issues and ongoing technological change imposed by the dynamic environment. The latter is driven by the rapid evolution and transformation of semiconductor products. Providing innovative manufacturing solutions and realizing opportunities that can be used to address increasing challenges for microelectronics manufacturing will require a collaborative interdisciplinary approach.

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NOMENCLATURE

193i	193 nm immersion (lithography)
2D	two-dimensional
3D	three-dimensions
AIMD	*ab-initio* molecular dynamics
ALD	atomic layer deposition
ALE	atomic layer etching
ARDE	aspect ratio dependent etching
ASD	area selective deposition
ATR-FTIR	attenuated total reflectance-Fourier transform infra-red
BEOL	back end of line
BTBAS	bis(T-butylamino)silane
CAR	chemically amplified resist
CCP	capacitively coupled plasma
CD	critical dimension
CDU	critical dimension unifrormity
CG	coarse-grained
CMOS	complementary metal–oxide–semiconductor
CoO	cost of ownership
CPU	central processing unit
CVD	chemical vapor deposition
CW	continuous wave
DC	direct current
DCS	direct current superimposed
DFT	density functional theory
DIPAS	di-isopropylamino silane
DMAC	dimethyl aluminum-chloride
DRAM	dynamic random-access memory
DRIE	deep-reactive ion etching
DUV	deep ultraviolet (typically 200–280 nm)
EADSet	evaluated and authorized dataset
EEDF	electron energy distribution function
EELS	electron energy loss spectroscopy
EES	equipped engineering system
EMI	electro-magnetic interference
EPC	etch per cycle
ER	etch rate
ESC	electro-static chuck
EUV	extreme ultraviolet
FDC	fault detection and classification
FET	field-effect transistor
finFET	fin-type field effect transistor
FTIR	Fourier transform infrared
GAA	gate-all-around
GCIB	gas cluster ion beam
GST	GeSbTe
HAADF	high angle annular dark field
HAR	high aspect ratio
HARC	high aspect ratio contacts
HPC	high-performance computing
HTS	high-throughput screening
HVM	high volume manufacturing
IADF	ion angular distribution function
IBE	ion beam etching
ICP	inductively coupled plasma
IDM	integrated device manufacturer
IEADF	ion energy and angle distribution function
IEDF	ion energy distribution function
IGZO	InGaZnO
ILD	interlayer dielectric
IRDS	international roadmap for devices and systems
L/S	line/space
LER	line edge roughness
LWR	line width roughness
MD	molecular dynamics
MLP	machine-learned potentials
MMP	mixed mode pulsing
MOSFET	metal–oxide–semiconductor field-effect transistor
MRAM	magnetic random-access memory
NA	numerical aperture
NAND	NOT AND
NC	negative capacitance
n-MOS	n-type doped MOS
OES	optical emission spectroscopy
ONON	oxide-nitride-oxide-nitride
OSG	organo silicate glass
PE	plasma etching
PID	plasma induced damage
p-MOS	p-type doped MOS
PR	photoresist
PVD	physical vapor deposition
RDL	redistribution layers
RF	radio frequency
RIE	lag reactive ion etching lag (smaller features etch at a slower rate than larger features)
RIE	reactive ion etching
S/D	source/drain
SAC	self-aligned contact
SADP	self-aligned double patterning
SALELE	aligned litho-etch litho-etch
SE	single exposure
STEM	scanning transmission electron microscope
TDDFT	time-dependent density functional theory
TDV	through-dielectric via
TEM	transmission electron microscope
TFT	thin film transistor
TOF-SIMS	time-of-flight secondary ion mass spectrometry
TSV	through-silicon via
TTT	In nano metrology, TTT is defined as distance between line ends, also known as tip-to-tip CD
VHF	very high frequency
VNAND	vertically (stacked) NAND
VPI	vapor phase infiltration
VUV	vacuum ultraviolet
WPE	wafer processing equipment
XPS	x-ray photoelectron spectroscopy

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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