YEON GEUN YOOK

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Email: ygyook@umich.edu

AREAS OF INTEREST

- Low Temperature Plasma / Plasma Modeling and Simulation
- Plasma Etching / Semiconductor Fabrication Process

EDUCATION

UNIVERSITY OF MICHIGAN, Ann Arbor, Michigan, USA **08/2023-Present**
Ph.D. Student, Electrical Engineering and Computer Science
- Advisor: Prof. Mark J. Kushner
  - Computational Plasma Science and Engineering Group
- Research Experience:
  - Modeling and analysis of plasma etching utilizing HPEM and MCFPM
  - Cryogenic etching, multi-frequency synchronous/asynchronous pulsed plasma, and matching network

YONSEI UNIVERSITY, Seoul, Republic of Korea **03/2010-02/2016**
B.S., Electrical and Electronic Engineering

WORK EXPERIENCE

SAMSUNG ELECTRONICS CO., LTD., Hwaseong, Republic of Korea **03/2016-Present**

***Staff Engineer*, Advanced Process Development Team, Semiconductor R&D Center** 03/2023-Present
Engineer, Advanced Process Development Team, Semiconductor R&D Center 01/2021-02/2023
- Duty: Advanced patterning etch process development
  - Development of V-NAND High Aspect Ratio Contact (HARC) channel hole etch processes utilizing cryogenic plasma etching, and various Middle-End of Line etch processes
  - Development of V-NAND Back-End of Line metallization etch processes for wafer bonding technology
  - Development of next-generation etch processes for advanced 3D DRAM technology
  - Development of etch emulator software to enhance process efficiency
- Notable achievement:
  - Development of cryogenic HARC etch processes with aspect ratios exceeding 70, including those surpassing 100, and establishment of conditions applicable to pioneering HARC-Merged structure designs
- External collaboration: LAM Research Co., Applied Materials Co., and Tokyo Electron Co.

Engineer, Flash Process Development Team, Semiconductor R&D Center 03/2016-12/2020
- Duty: Flash memory etch processes and advanced patterning development
  - Development of V-NAND HARC channel hole etch processes utilizing cryogenic and conventional etching
  - Development of HARC amorphous carbon layer (ACL) mask etch processes
  - Development of V-NAND word-line formation and transistor formation processes
  - Development of V-NAND various Front-End of Line etch processes
- Notable achievement:
  - Establishment of reaction mechanisms based on process parameter variations and HARC etch process conditions using cryogenic plasma
  - Innovations in word-line formation and other Front-End of Line processes through process improvements, result in significant reductions in production costs
- External collaboration: LAM Research Co., Applied Materials Co., and Tokyo Electron Co.

SAMSUNG ELECTRONICS CO., LTD., Hwaseong, Republic of Korea **01/2015-02/2015**

Intern, Advanced Equipment Development Project Team, Semiconductor R&D Center
- Investigation of uniformity improvement of metal contact patterns

AWARDS & HONORS

2023 Samsung Best Paper Awards, Bronze Award, Samsung Groups	09/2023
International Academic Training Fellowship: Full-Ride Scholarship Finalist funded by Samsung Electronics	10/2022
2021 SRD e-Technical Journal Junior Paper Award, Samsung Electronics	01/2022
Monthly Process Development Team Immediate Award, Samsung Electronics	five times
Academic Scholarship, Yonsei University	08/2010

PATENTS

4. Y. S. Lee, **Y. G. Yook**, and H. Kim, *Semiconductor Device and Electronic System Including the Same,* Korea – Application No. P20220026988, US – Application No. US18/097332, and China – Application No. 202310177405.1 (2022)

3. **Y. G. Yook**, H. Kim, and Y. S. Lee, *Three-Dimensional Semiconductor Memory Device and Electronic System Including the Same*, Korea – Application No. P20210188760, US – Application No. US18/080325, and China – Application No. 202211641903.9 (2021)

2. J. Y. Park, H. Kim, **Y. G. Yook**, and Y. S. Lee, *Semiconductor Memory Devices, Electronic Systems including the Same, and Fabricating Methods of the Same,* Korea – Application No. P20210154857, US – Application No. US17/819330, and China – Application No. 202211409023.9 (2021)

1. J. Y. Park, H. Kim, and **Y. G. Yook**, *Semiconductor Device Including Channel Structure and Flow-Through Electrodes, Electronic System, and Method of Forming the Same,* Korea – Application No. P20210116688, US – Application No. US17/693328, and China – Application No. 202211064994.4 (2021)

SAMSUNG INTERNAL PAPERS *(Not published)*

4. K. S. Chung, **Y. G. Yook**, and G. W. Kim, *Cutting-edge HARC Merge Scheme of VNAND Memory using Cryogenic Etching Challenges and Solutions,* Samsung Best Paper Awards 2023 (2023)

3. K. S. Chung, **Y. G. Yook**, G. W. Kim, H. Kim, and S. W. Park, *Feasibility Study of Cryogenic Etch in HARC Merge Scheme with Hole-type Cut*, SRD e-Technical Journal 2022 2nd Half (2022)

2. **Y. G. Yook**, Y. S. Lee, K. S. Chung, H. Kim, and S.W. Park, *Dry Etch Characteristics of Oxide Film Using Ch. Hole Etch Process for the HARC MERGE Structure,* SRD e-Technical Journal 2021 2nd Half (2021)

1. **Y. G. Yook**, Y. T. Jee, H. Kim, and J. H. Yoo, *A Study on the Characteristics of Halogen Radical Effect in Cryogenic Etch Process for HARC in V-NAND Devices*, SRD e-Technical Journal 2020 1st Half (2020)

PRESENTATIONS

8. **Y. G. Yook**, and M. J. Kushner, *Mechanisms for Cryogenic Plasma Etching of SiO_2,* AVS 2024 (American Vacuum Society), Tampa, Florida, USA (2024)

7. **Y. G. Yook**, and M. J. Kushner, *Strategic Integration of RF Pulsing in Multi-Frequency CCPs for Dielectric HARC Etching and its Applications,* Technical Workshop 2024, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2024)

6. **Y. G. Yook**, *Methods about Plasma Edge Strip for Defect Control and Grounding in V-NAND,* V-NAND Etch Research Group, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2022)

5. **Y. G. Yook**, *Line and Contact Etch Processes in the Merged Structure of All HARC Processes,* Advanced Patterning Photo & Etch Technology Seminar, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2021)

4. **Y. G. Yook**, *Analysis and Understanding of Channel Hole HARC Etch Process Using Cryogenic Plasma Etching,* Advanced Patterning Photo & Etch Technology Seminar, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2021)

3. **Y. G. Yook**, *Reaction Mechanisms of Various Process Parameters in HARC Etch Process Using Cryogenic Plasma Etching,* Cryogenic Plasma Etch Research Group, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2020)

2. **Y. G. Yook**, *Analysis of Challenging Deep Channel Hole Etch Process Evaluation Results,* Cryogenic Plasma Etch Research Group, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2020)

1. **Y. G. Yook**, *Development History of V-NAND Front-End of Line Processes,* V-NAND FEOL Process Transfer Seminar, Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea (2020)

POSTER PRESENTATIONS

2. **Y. G. Yook**, and M. J. Kushner, *Mechanisms for Cryogenic Plasma Etching of SiO_2,* 15th MIPSE Graduate Symposium 2024, University of Michigan, Ann Arbor, Michigan, USA (2024)

1. **Y. G. Yook**, and M. J. Kushner, *Strategic Integration of RF Pulsing in Multi-Frequency CCPs for Dielectric HARC Etching,* GRS 2024 (Gordon Research Seminar), Andover, New Hampshire, USA (2024)

ACTIVITIES

Participant, 2nd US Low Temperature Plasma Summer School, University of Michigan	06/2023
Selected Freshman Trainer, Samsung Job Mentoring and Recruitment, Samsung Electronics	09/2021
Selected Freshman Trainer, Samsung Shared Value Program for new employees, Samsung Groups	11/2020-01/2021
Participant, 2300 System, SW Operation, and Qualification Seminar, LAM Research	01/2019
Volunteer, Mentoring Services of Hope Fellowship for Geoje High School, Yonsei University	02/2014

MILITARY SERVICE

REPUBLIC OF KOREA AIR FORCE, Gyeonggi-do, Republic of Korea 06/2011-06/2013
Discharged as a Sergeant, 15th Special Missions Wing